1 Features

- Supports MIPI Alliance Specification for D-PHY Version 2.5
- Consists of 1 Clock lane and 2 Data lanes in D-PHY mode
- 80 Mbps to 1.2 Gbps data rate per lane in high-speed D-PHY mode
- Supports LVDS compatible with TIA/EIA-644 standard
- Consists of 3 channels in LVDS mode
- 600 Mbit/s/channel in LVDS mode
- Supports both 8-bit serial data and 10-bit serial data for LVDS
- LVDS current configurable
- Embedded, high performance, and highly programmable PLL
- PLL has 2 independent dividers at the output of the VCO: one divider for core circuits and one for MIPI. The 2 dividers have independent settings of division factor.
- Supports both low-power mode and high-speed mode with integrated SERDES
- 10 Mbps data rate in D-PHY low-power mode
- Low power dissipation
- Supports operation with reduced amount of data lanes. Unused data lanes can be put in power-down mode in which all current paths shall be cut and no current shall flow.
- Testability support

2 General Description

The MXL-LVDS-D-PHY-CSITX-TW-65BSB is a high-frequency, low-power, low-cost, source-synchronous, physical Layer supporting the MIPI Alliance Specification for D-PHY v2.5 and LVDS compatible with TIA/EIA-644 standard and. The PHY can be configured as a MIPI Master supporting camera interface CSI-2. The PHY supports mobile, IoT, virtual reality, and automotive applications.

3 Block Diagram