# 1 Features

- Consists of 1 Clock lane and up to 4 Data lanes
- Supports MIPI Standard 2.1 for D-PHY
- Supports both high speed and low-power modes
- 80 Mbps to 1.2Gbps data rate in high speed mode
- 10 Mbps data rate in low-power mode
- High Speed Serializer included
- Low power dissipation

# 2 General Description

The MXL-DPHY-CSI2-TX is a high-frequency low-power, low-cost, source-synchronous, Physical Layer supporting the MIPI Alliance Standard for D-PHY. The IP is configured as a MIPI master optimized for camera interface applications (CSI-2).

The High-Speed signals have a low voltage swing, while Low-Power signals have large swing. High-Speed functions are used for High-Speed data traffic while low power functions are mostly used for control.

# 3 Block Diagram

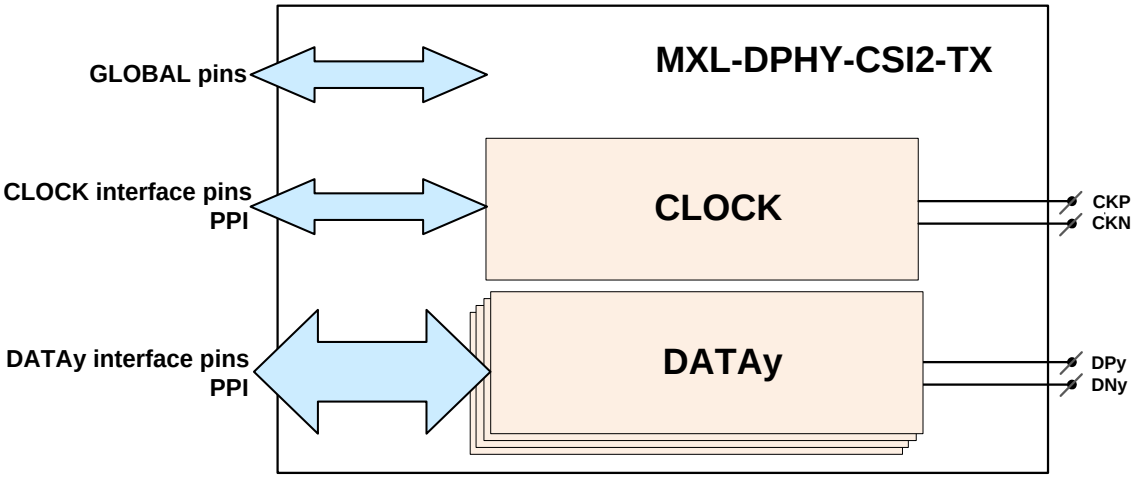


**Figure 1: MIPI D-PHY CSI-2-TX Block Diagram**