1 Features

- Consists of 1 Clock lane and up to 4 Data lanes.
- Supports MIPI® Alliance Specification for D-PHY℠ Version 1.1.
- Supports both high speed and low-power modes.
- 80 Mbps to 1.5 Gbps data rate in high speed mode.
- 10 Mbps data rate in low-power mode.
- High Speed Serializers and Deserializers included.
- Low power dissipation.
- Loopback testability support.
- Optional resistance termination calibrator.

2 General Description

The MXL-DPHY-UNIV is a high-frequency low-power, low-cost, source-synchronous, Physical Layer supporting the MIPI Alliance Specification for D-PHY v1.1.
The IP can be configured as a MIPI Master or MIPI Slave optimized for CSI-2℠ (Camera Serial Interface), and DSI℠ (Display Serial Interface) applications.
The High-Speed signals have a low voltage swing, while Low-Power signals have large swing. High-Speed functions are used for High-Speed data traffic while low power functions are mostly used for control.

3 Block Diagram

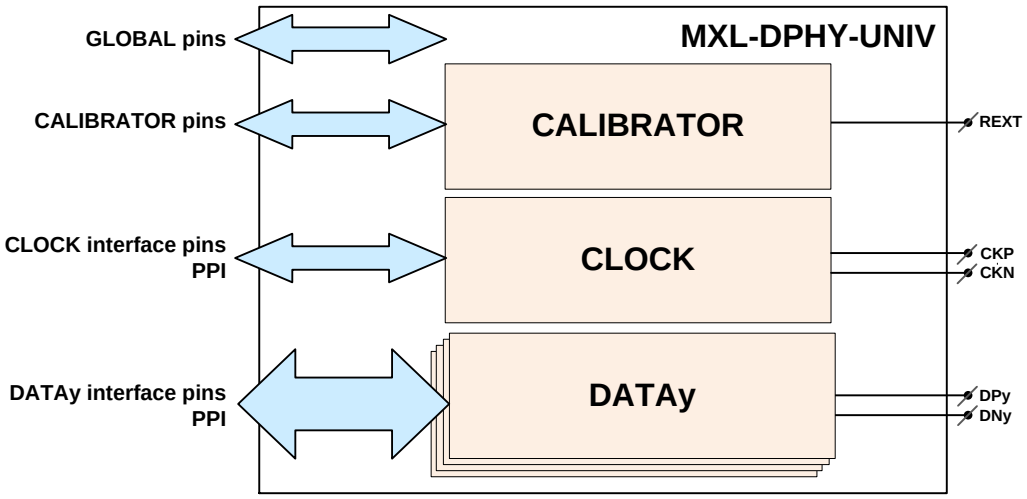

Figure 1: MIPI D-PHY Universal Block Diagram

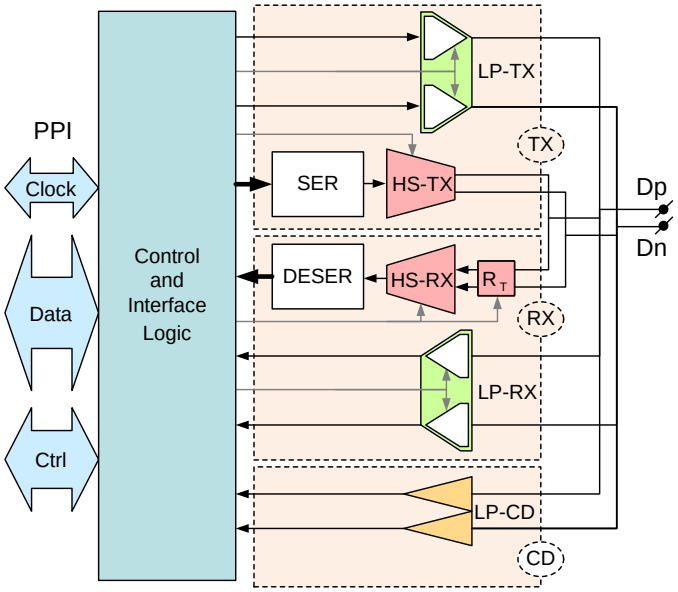

Figure 2: Universal Lane Overview