1 Features

- Dual mode PHY Supports MIPI Alliance Specification D-PHY v2.5 & C-PHY v2.0
- Consists of 1 Clock lane and 4 Data lanes in D-PHY mode
- Consists of 3 Data lanes in C-PHY mode
- Embedded, high performance, and highly programmable PLL
- PLL supports SSC mode, Fractional mode, and Integer mode
- Supports both low-power mode and high speed mode with integrated SERDES
- 80 Mbps to 1.5 Gbps data rate per lane without skew calibration in D-PHY mode
- 4.5 Gbps data rate per lane with skew calibration in high speed D-PHY mode
- 80 Msps to 3.5 Gsps symbol rate per lane in high speed C-PHY mode
- Supports High Speed TX De-emphasis Equalization
- 10 Mbps data rate in low-power mode
- Low power dissipation
- Testability support including internal loopback
- Calibrator for resistance termination

2 General Description

The MXL-CD-PHY-DSITX+-T-N05 is a high-frequency, low-power, low-cost, source-synchronous, physical Layer supporting the MIPI Alliance Specification for D-PHY v2.5 and C-PHY v2.0. The PHY can be configured as a MIPI Master supporting display interface DSI/DSI-2. The PHY supports mobile, IoT, virtual reality, and automotive applications. The DSI TX+ is a Mixel proprietary configuration that is optimized to support full-speed production and in-system testing while minimizing area and leakage power.

3 Block Diagram

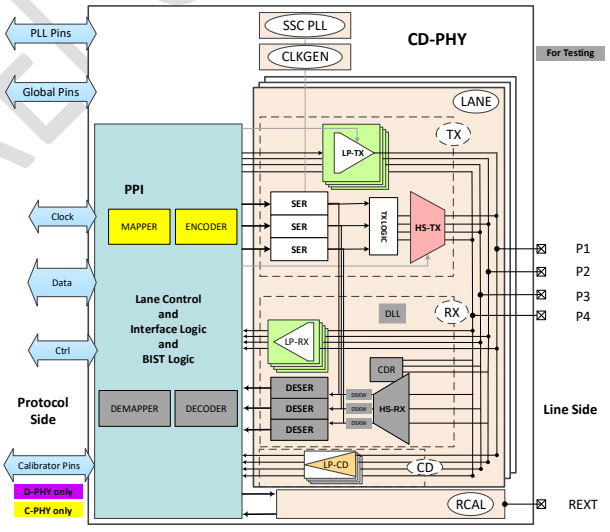

Figure 3-1: MIPI CD-PHY Block Diagram