1 Features

- Supports MIPI Alliance Specification for D-PHY Version 2.5
- Consists of 1 Clock lane and 4 Data lanes
- Embedded, high performance, and highly programmable PLL
- Supports both low-power mode and high speed mode with integrated SERDES
- 80 Mbps to 1.5 Gbps data rate per lane without skew calibration in D-PHY mode
- 2.56 Gbps data rate per lane with skew calibration in high speed D-PHY mode
- 10 Mbps data rate in low-power mode
- Low power dissipation
- Testability support including internal loopback
- Calibrator for resistance termination

2 General Description

The MXL-D-PHY-UNIV-T-28HPCP is a high-frequency, low-power, low-cost, source-synchronous, physical Layer supporting the MIPI Alliance Specification for D-PHY v2.5. The PHY can be configured as a MIPI Master or MIPI Slave supporting camera interface CSI-2 and display interface DSI/DSI-2. The PHY supports mobile, IoT, virtual reality, and automotive applications.

3 Block Diagram

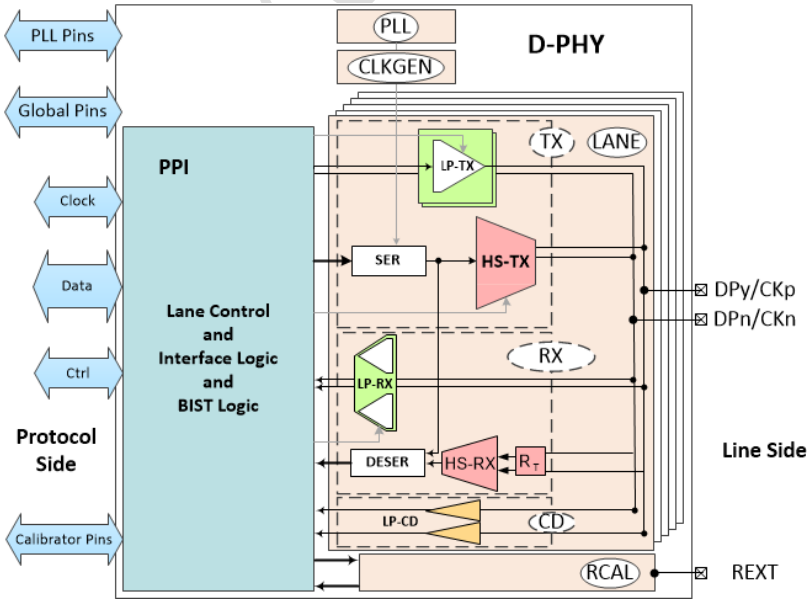

Figure 3-1: MIPI D-PHY Block Diagram