1 Features

DPHY

- Consists of 1 Clock lane and up to 4 Data lanes
- Supports MIPI® Alliance Specification for D-PHY Version 2.1
- Supports both high speed and low-power modes
- 80 Mbps to 1.5 Gbps data rate per lane in D-PHY mode
- 10 Mbps data rate in low-power mode
- Low power dissipation
- Testability support

LVDS

- 75MHz in 8 bits mode and 85.7MHz in 7 bits mode clock support
- Consists of 1 Clock lane and up to 4 Data lanes
- Up to 0.6 Gbps per lane
- Up to 2.4 Gbps data throughput
- 7/8 bit programmable serial data transmitted per pixel clock per cannel

2 General Description

The MXL-LVDS-DPHY-CSI2-RX is a high-frequency low-power, low-cost, source-synchronous, Physical Layer supporting the MIPI Alliance Specification for D-PHY v2.1, which is backward compatible with MIPI Specification for D-PHY v1.2. The IP is configured as a MIPI Slave optimized for CSI-2℠ (Camera Serial Interface) applications. The High-Speed signals have a low voltage swing, while Low-Power signals have large swing. High-Speed functions are used for High-Speed data traffic while low power functions are mostly used for control.

The MXL-LVDS-DPHY-CSI2-RX is a high performance 4-channel LVDS Receiver implemented using digital CMOS technology. Both the serial and parallel data are organized into four channels. The parallel data can be 7 or 8 bits wide per channel. The input clock frequency is up to 75MHz or 85.7MHz. The Receiver is highly integrated and requires no external components. Great care was taken to ensure matching between the Data and Clock channels to maximize the receiver margin. The circuit is designed in a modular fashion and desensitized to process variations. This facilitates process migration, and results in a robust design.