

## 1 Features

- Dual mode PHY Supports MIPI Alliance Specification D-PHY v2.5 & C-PHY v2.0
- Consists of 1 Clock lane and 4 Data lanes in D-PHY mode
- Consists of 3 Data lanes in C-PHY mode
- Supports both low-power mode and high speed mode with integrated SERDES
- 80 Mbps to 1.5 Gbps data rate per lane without skew calibration in D-PHY mode
- 2.5 Gbps data rate per lane with skew calibration in high speed D-PHY mode
- 80 Msps to 2.5 Gsps symbol rate per lane in high speed C-PHY mode
- 10 Mbps data rate in low-power mode
- Low power dissipation
- Testability support

## 2 General Description

The MXL-CD-PHY-DSIRX-T-22ULP is a high-frequency, low-power, low-cost, source-synchronous, physical Layer supporting the MIPI Alliance Specification for D-PHY v2.5 and C-PHY v2.0. The PHY can be configured as a MIPI Slave supporting display interface DSI/DSI-2. The PHY supports mobile, IoT, virtual reality, and automotive applications.

## 3 Block Diagram

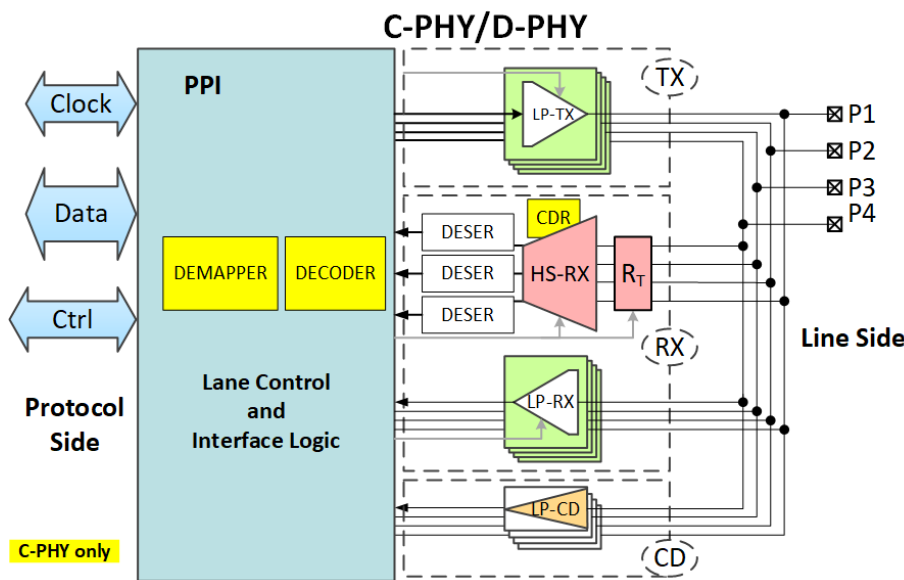


Figure 3-1: MIPI CD-PHY Block Diagram