1 Features

- Supports MIPI Alliance Specification for D-PHY Version 2.5
- Consists of 1 Clock lane and 1 Data lanes
- Embedded, high performance, and highly programmable PLL
- Supports both low-power mode and high speed mode with integrated SERDES
- 80 Mbps to 1.5 Gbps data rate per lane in high speed D-PHY mode
- 10 Mbps data rate in low-power mode
- Low power dissipation
- Testability support

2 General Description

The MXL-D-PHY-CSITX-T-22ULL is a high-frequency, low-power, low-cost, source-synchronous, physical Layer supporting the MIPI Alliance Specification for D-PHY v2.5. The PHY can be configured as a MIPI Master supporting camera interface CSI-2. The PHY supports mobile, IoT, virtual reality, and automotive applications.
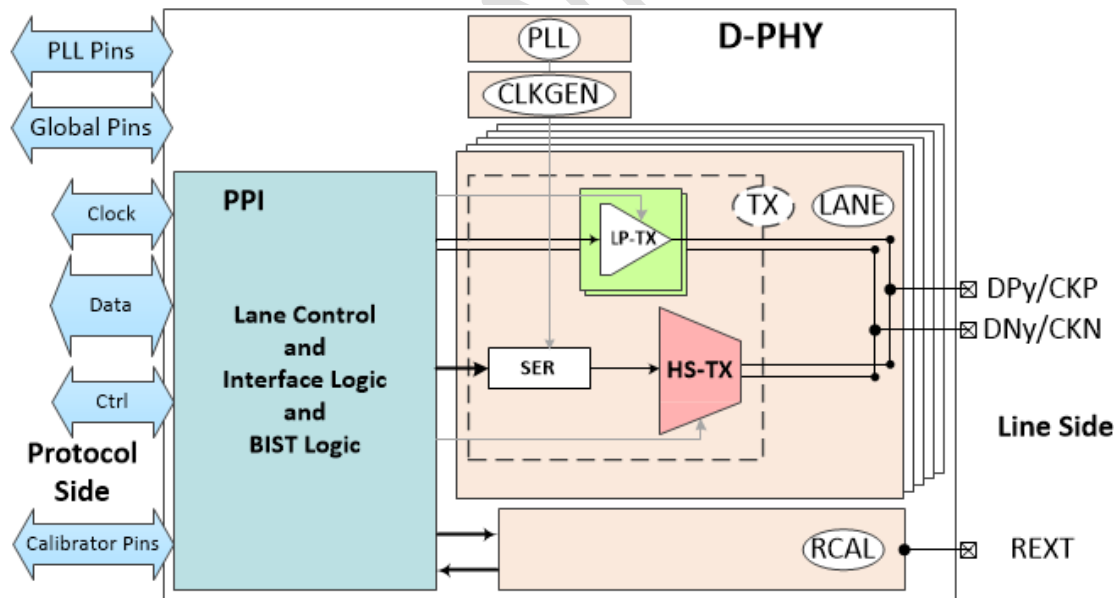
3 Block Diagram

Figure 3-1: MIPI D-PHY Block Diagram

Figure 3-1 shows the top-level block diagram of the MXL-D-PHY-CSITX-T-22ULL IP. It consists of a Clock Lane Module and up to four Data Lane Modules, and is targeting

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