1 Features

- Supports MIPI Alliance Specification for D-PHY Version 2.1
- Consists of 1 Clock lane and 4 Data lanes
- Embedded, high performance, and highly programmable PLL
- Supports both low-power mode and high speed mode with integrated SERDES
- 80 Mbps to 1.5 Gbps data rate per lane in high speed D-PHY mode
- 10 Mbps data rate in low-power mode
- Low power dissipation
- Testability support including internal loopback

2 General Description

The MXL-D-PHY-CSITX+-T-40ULP is a high-frequency, low-power, low-cost, source-synchronous, physical Layer supporting the MIPI Alliance Specification for D-PHY v2.1. The PHY can be configured as a MIPI Master supporting camera interface CSI-2. The PHY supports mobile, IoT, virtual reality, and automotive applications. The CSI-2 TX+ is a Mixel proprietary configuration that is optimized to support full-speed production and in-system testing while minimizing area and leakage power.

3 Block Diagram

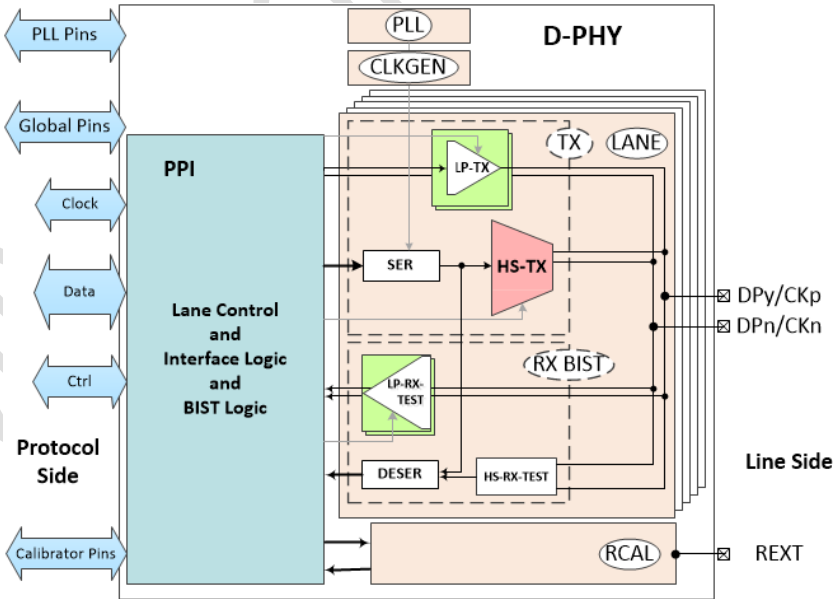

Figure 3-1: MIPI D-PHY Block Diagram

Figure 3-1 shows the top-level block diagram of the MXL-D-PHY-CSITX+-T-40ULP IP. It consists of a Clock Lane Module and up to four Data Lane Modules, and is targeting maximum rate of 1.5 Gbps. In addition to the lanes, the IP may include an optional calibrator module for calibration of termination resistance. Each of these PHY Lane Modules communicates through a differential line to a complementary PHY at the other side of the lane interconnect.

The D-PHY supports MIPI Specification for D-PHY Version 2.1, which is backward compatible with MIPI Specifications for D-PHY v1.2, and D-PHY v1.1.

MXL-D-PHY-CSITX+-T-40ULP is partitioned into a Digital Module - CIL (Control and Interface Logic) and a Mixed Signal Module. The PHY system is provided as a combination of Soft IP views (RTL, and STA Constraints) for Digital Module, and Hard IP views (GDSII/CDL/LEF/LIB) for the Mixed Signal Module. This unique offering of Soft and Hard IP permits architectural design flexibility and seamless implementation in customer-specific design flow.

The CIL module interfaces with the Protocol and determines the global operation of the Lane Module. The interface between the PHY and the protocol is called the PHY-Protocol Interface (PPI).

The Mixed Signal Module includes High-Speed signaling mode for fast-data traffic and Low-Power signaling mode for control purposes. DATAy are unidirectional lanes and consist of High-Speed Transmitter (HS-TX), Low-Power Transmitter (LP-TX), and Serializer (SER). D-PHY CLOCK lane is a unidirectional lane and consists of High-Speed Transmitter (HS-TX), and Low-Power Transmitter (LP-TX). Module RCAL is optional and is used to calibrate the HS-TX termination, which requires connecting the pin REXT with a precise external resistor.

During normal operation, a Lane switches between Low-Power and High-Speed mode. Bidirectional Lanes can also switch communication direction. The change of operating mode or direction requires enabling and disabling of certain electrical functions. These enable and disable events do not cause glitches on the Lines that would result in a detection of an incorrect signal level. Therefore, all mode and direction changes are smooth to always ensure a proper detection of the Line signals.