1 Features

- Supports MIPI® Specification for D-PHY Version 2.1.
- Consists of 1 Clock lane and up to 4 Data lanes.
- Supports both high speed and low-power modes.
- 80 Mbps to 1.5 Gbps data rate per lane without Deskew calibration.
- Up to 2.5 Gbps data rate per lane with Deskew calibration.
- 10 Mbps data rate in low-power mode.
- Low power dissipation.
- Loopback testability support.
- Optional resistance termination calibrator.
- Deskew calibration support.

2 General Description

The MXL-DPHY-UNIV is a high-frequency low-power, low-cost, source-synchronous, physical Layer. The PHY can be configured as a MIPI Master or MIPI Slave supporting camera interface CSI-2 v1.2 and display interface DSI v1.3 applications. The High-Speed signals have a low voltage swing, while Low-Power signals have large swing. High-Speed functions are used for High-Speed data traffic while low power functions are mostly used for control.

The D-PHY supports a bit rate range of 80 to 1500 Mbps per Lane without deskew calibration and up to 2500 Mbps with deskew calibration.

To minimize EMI, the drivers for low-power mode are slew-rate controlled and current limited. The maximum data rate in low-power mode is 10 Mbps. For a fixed clock frequency, the available data capacity of a PHY configuration can be increased by using more lanes. Effective data throughput can be reduced by employing burst mode communication.

3 Block Diagram

The block diagram for D-PHY are shown in Figure 1 and Figure 2

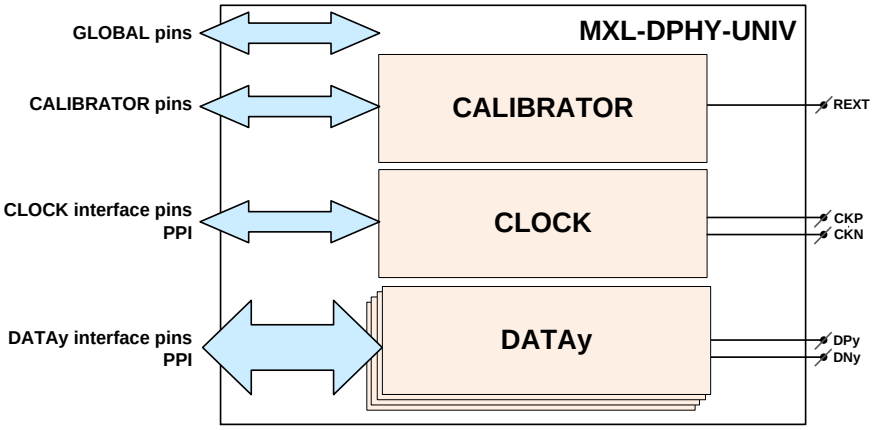

Figure 1: MIPI D-PHY Universal Block Diagram

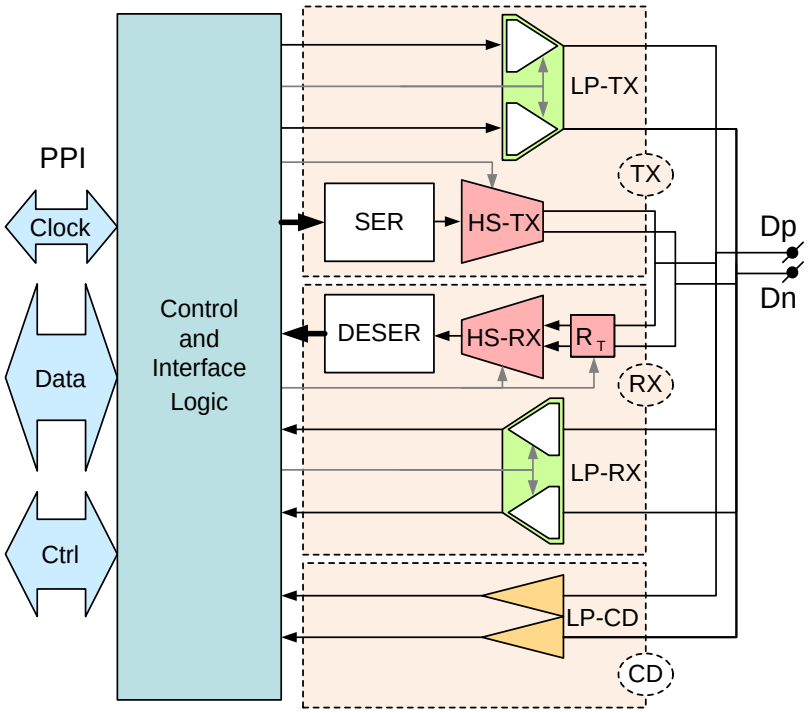

Figure 2: D-PHY Universal Lane Overview