1 Features

DPHY:

- Consists of 1 Clock lane and up to 4 Data lanes
- Supports MIPI Standard 1.1 for D-PHY
- Supports both high speed and low-power modes
- 80 Mbps to 1.05Gbps data rate in high speed mode
- 10 Mbps data rate in low-power mode
- High Speed Serializer included
- Low power dissipation
- Optional resistance termination calibrator

LVDS:

- 24-150 MHz clock support
- Up to 1050 Mbps bandwidth/channel
- Up to 4.2 Gbps data throughput
- Low power CMOS design
- LVDS for low EMI
- PLL requires no external components
- Core Voltage & 1.8V dual power supply
- 7 bit serial data transmitted per pixel clock per channel
- Rising/falling edge data strobe
- Compatible with TIA/EIA-644 LVDS Standard

2 General Description

The MXL-LVDS-DPHY-DSI-TX is a combo PHY that consists of a high-frequency low-power, low-cost, source-synchronous, Physical Layer supporting the MIPI Alliance Standard for D-PHY and a high performance 4-channel LVDS Serializer implemented using digital CMOS technology.
In D-PHY mode, The IP can be configured as a MIPI Master optimized for display (DSI) applications. The High-Speed signals have a low voltage swing, while Low-Power signals have large swing. High-Speed functions are used for High-Speed data traffic while low power functions are mostly used for control.
In LVDS mode, both the serial and parallel data are organized into 4 channels. The parallel data is 7 bits wide per channel. The input clock is 25MHz to 150MHz. The serializer is highly integrated and requires no external components. The circuit is designed in a modular fashion and desensitized to process variations. This facilitates process migration, and results in a robust design.

3 Block Diagram

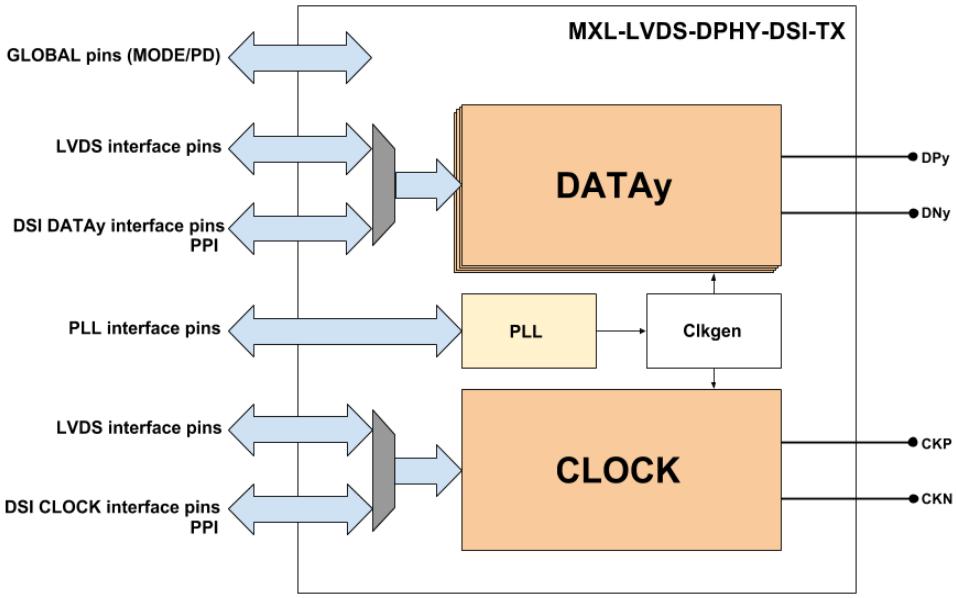

Figure 1:MIPI D-PHY DSI-TX/LVDS-TX Block Diagram