

1 Features

- Supports MIPI Alliance Specification for D-PHY Version 2.1
- Backward compatible with MIPI Specifications for D-PHY v1.2, and v1.1
- Consists of 1 Clock lane and 4 Data lanes
- Embedded high performance, highly programmable, PLL
- Supports both high speed and low-power modes
- 80 Mbps to 1.5 Gbps data rate per lane without Deskew calibration
- Up to 2.5 Gbps data rate per lane with Deskew calibration
- 10 Mbps data rate in low-power mode
- Low power dissipation
- Testability support including internal loopback
- Calibrator for resistance termination

2 General Description

The MXL-D-PHY-UNIV-T-65GP is a high-frequency, low-power, low-cost, source-synchronous, physical Layer supporting the MIPI Alliance Specification for D-PHY v2.1. The PHY can be configured as a MIPI Master or MIPI Slave supporting camera interface CSI-2 and display interface DSI/DSI-2 applications.

3 Block Diagram

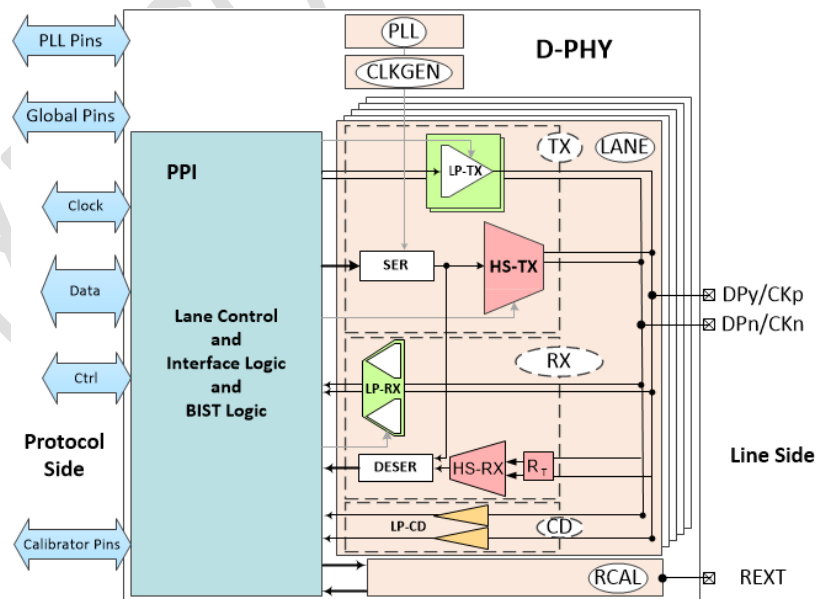


Figure 3-1: MIPI D-PHY Block Diagram