1 Features

- Supports MIPI Alliance Specification for D-PHY Version 2.5
- Backward compatible with MIPI Specifications for D-PHY v2.1, v1.2, and v1.1
- Consists of 1 Clock lane and 4 Data lanes
- Embedded high performance, highly programmable, PLL
- PLL supports SSC mode, Fractional mode, and Integer mode
- Supports both high speed and low-power modes
- Up to 4.5 Gbps data rate per lane with Deskew calibration
- Supports High Speed TX De-emphasis Equalization
- Supports High Speed RX CTLE
- 10 Mbps data rate in low-power mode
- Low power dissipation
- Testability support including internal loopback
- Calibrator for resistance termination

2 General Description

The MXL-D-PHY-UNIV-T-22ULP is a high-frequency, low-power, low-cost, source-synchronous, physical Layer supporting the MIPI Alliance Specification for D-PHY v2.5. The PHY can be configured as a MIPI Master or MIPI Slave supporting camera interface CSI-2 and display interface DSI/DSI-2 applications.

3 Block Diagram

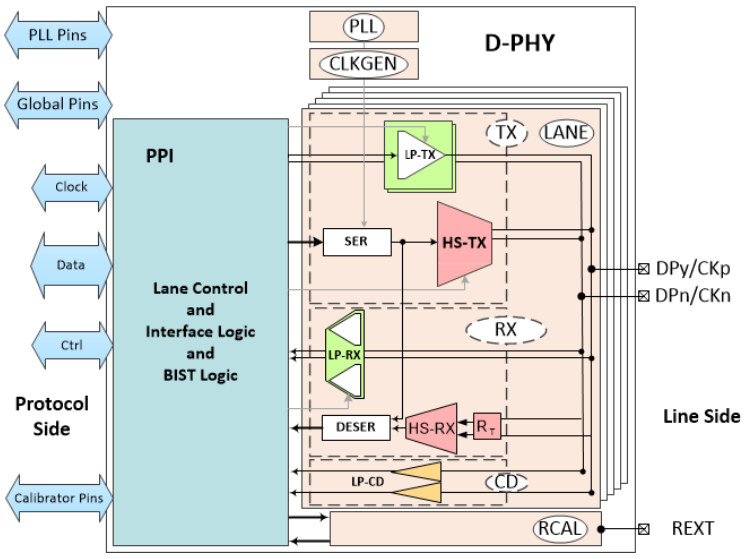

Figure 3-1: MIPI D-PHY Block Diagram

Figure 3-1 shows the top-level block diagram of the MXL-D-PHY-UNIV-T-22ULP IP. It consists of a Clock Lane Module and up to four Data Lane Modules. In addition to the lanes, the IP may include an optional calibrator module for calibration of termination resistance. Each of these PHY Lane Modules communicates through a differential line to a complementary PHY at the other side of the lane interconnect.
MXL-D-PHY-UNIV-T-22ULP is partitioned into a Digital Module - CIL (Control and Interface Logic) and a Mixed Signal Module. The D-PHY system is provided as a combination of Soft IP views (RTL, and STA Constraints) for Digital Module, and Hard IP views (GDSII/CDL/LEF/LIB) for the Mixed Signal Module. This unique offering of Soft and Hard IP permits architectural design flexibility and seamless implementation in customer-specific design flow.

The CIL module interfaces with the Protocol and determines the global operation of the Lane Module. The interface between the D-PHY and the protocol is called the PHY-Protocol Interface (PPI).

The Mixed Signal Module includes High-Speed signaling mode for fast-data traffic and Low-Power signaling mode for control purposes. DATAy are bidirectional lanes and consist of High-Speed Receiver (HS-RX), Low-Power Receiver (LP-RX), High-Speed Transmitter (HS-TX), Low-Power Transmitter (LP-TX), Low- Power Contention Detector (LP-CD), Serializer (SER) and De-Serializer (DESER). CLOCK lane is a bidirectional lane and consists of High-Speed Receiver (HS-RX), Low-Power Receiver (LP-RX), High-Speed Transmitter (HS-TX), and Low-Power Transmitter (LP-TX). Module RCAL is optional and is used to calibrate the HS-TX and HS-RX termination, which requires connecting the pin REXT with a precise external resistor.

During normal operation, a Lane switches between Low-Power and High-Speed mode. Bidirectional Lanes can also switch communication direction. The change of operating mode or direction requires enabling and disabling of certain electrical functions. These enable and disable events do not cause glitches on the Lines that would result in a detection of an incorrect signal level. Therefore, all mode and direction changes are smooth to always ensure a proper detection of the Line signals.