Mixed-Signal Excellence

Features:

- Consists of 1 Clock lane and 4 Data lanes
- Supports the MIPI Standard 1.1 for D-PHY^{SM}
- Supports both high speed and low-power modes
- 80 Mbps to 1.0Gbps data rate in high speed mode
- 10 Mbps data rate in low-power mode
- High Speed Serializer and De-Serializer included
- Low power dissipation

General Description:

The MXL-DPHY-UNIVERSAL-S-130 is a high-frequency low-power, low-cost, source-synchronous, Physical Layer that supports the MIPI® Alliance Standard for D-PHY.

The IP can be configured as a MIPI master or slave and consists of 5 lanes: 1 Clock lane and 4 data lanes.

The High-Speed signals have a low voltage swing, while Low-Power signals have large swing. High-Speed functions are used for High-Speed Data traffic while low power functions are mostly used for control.
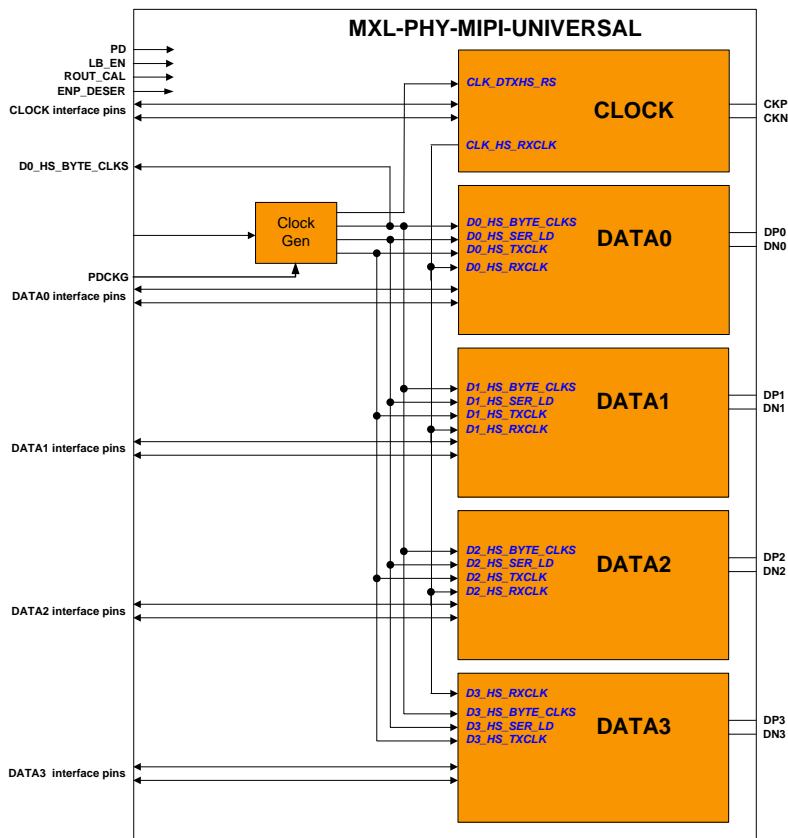
Block Diagram:

Figure 1 – PHY Block Diagram

Preliminary information

Subject to change Without notice

Proprietary & Confidential

Mixel, Inc.

97 E. Brokaw Road, Suite 250, San Jose, CA 95112

Ph.: (408) 436-8500, Fax: (408) 436-8400

www.mixel.com

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