

## 1 Features

- Supports MIPI Specification for C-PHY Version 1.1
- 80 Msps to 2.5 Gsps data rate in high speed mode
- Consists of One Lane
- 10 Mbps data rate in low-power mode
- Low power dissipation
- Testability support

## 2 General Description

The MXL-CPHY-CSI2-TX+ is a high-frequency low-power, low-cost, source-synchronous, physical Layer. The PHY is configured as a MIPI Master supporting camera interface CSI-2. The High-Speed signals have a low voltage swing, while Low-Power signals have large swing. High-Speed functions are used for High-Speed data traffic while low power functions are mostly used for control.

## 3 Block Diagram

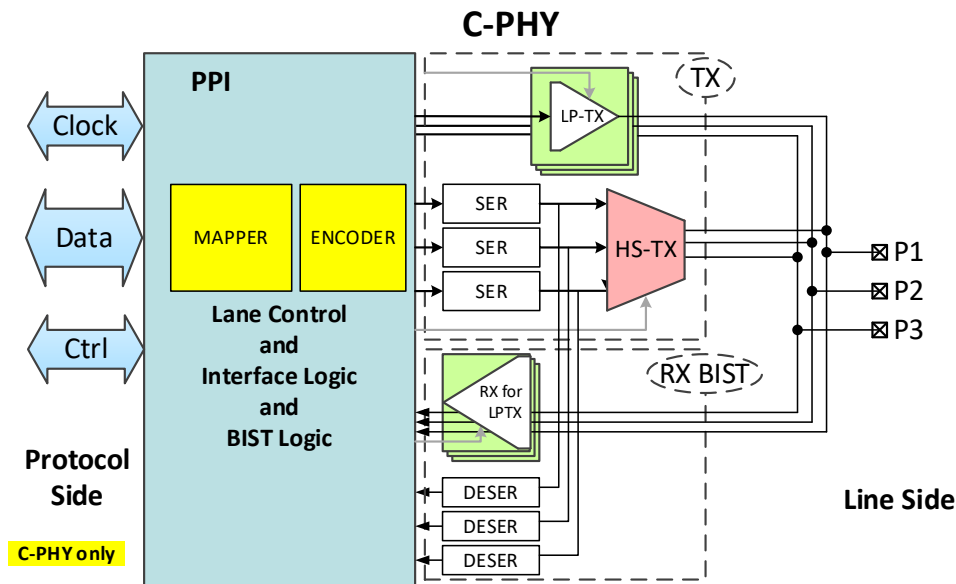


Figure 1: C-PHY TX+ Overview

The block diagram for C-PHY is shown in Figure 1, It supports MIPI Specification for C-PHY Version 1.1, which is backward compatible with MIPI Specification for C-PHY Version 1.0.



The C-PHY configuration consists of one lane modules which communicates via three lines to a complementary part at the other side of the lane interconnect. The C-PHY is based on 3-Phase symbol encoding technology delivering 2.28 bits per symbol over three-wire trios, and is targeting maximum rate of 2.5 Gsymbols/s.

MXL-CPHY-CSI2-TX+ is partitioned into a Digital Module - CIL (Control and Interface Logic) and a Mixed Signal Module. The PHY system is provided as a combination of Soft IP views (RTL, and STA Constraints) for Digital Module, and Hard IP views (GDSII/CDL/LEF/LIB) for the Mixed Signal Module. This unique offering of Soft and Hard IP permits architectural design flexibility and seamless implementation in customer-specific design flow.

The CIL module interfaces with the Protocol and determines the global operation of the Lane Module. The interface between the PHY and the protocol is using the PHY-Protocol Interface (PPI). The Mixed Signal Module includes High-Speed signaling mode for fast-data traffic and Low-Power signaling mode for control purposes.

During normal operation, a Lane switches between Low-Power and High-Speed mode. Bidirectional Lanes can also switch communication direction. The change of operating mode or direction requires enabling and disabling of certain electrical functions. These enable and disable events do not cause glitches on the Lines that would result in a detection of an incorrect signal level. Therefore, all mode and direction changes are smooth to always ensure a proper detection of the Line signals.