1 Features

- Consists of 1 Clock lane and up to 4 Data lanes
- Supports MIPI® Alliance Specification for D-PHY Version 2.1
- Supports both high speed and low-power modes
- 80 Mbps to 2.5Gbps data rate in high speed mode
- 10 Mbps data rate in low-power mode
- Low power dissipation
- Embedded PLL

2 General Description

The MXL-DPHY-CSI2-TX is a high-frequency low-power, low-cost, source synchronous, Physical Layer supporting the MIPI Alliance Specification for D-PHY v2.1, which is backward compatible with MIPI Specification for D-PHY v1.2. The IP is configured as a MIPI master optimized for CSI-2^{SM} (Camera Serial Interface) applications.
The High-Speed signals have a low voltage swing, while Low-Power signals have large swing. High-Speed functions are used for high-Speed data traffic while low power functions are mostly used for control. The embedded PLL is highly integrated and requires no external components. The PLL incorporates a lock detector, one independent output divider and supports full power down modes. Differential circuit techniques are employed to attain low jitter in the noisy environment typical of multi-million gates digital chip. The circuit is designed in a modular fashion and desensitized to process variations.

3 Block Diagram

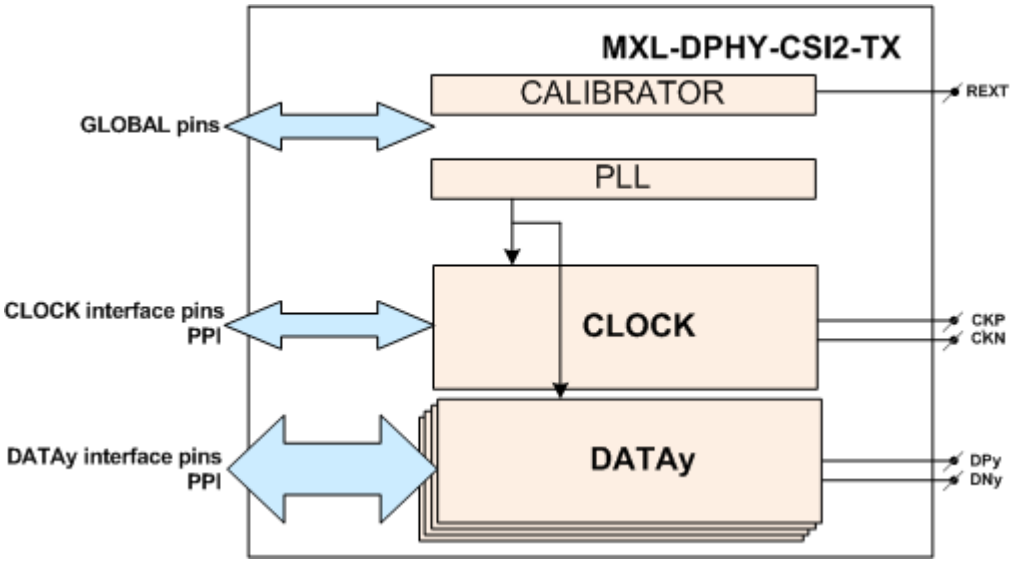

Figure 1: MIPI D-PHY CSI-2-TX Block Diagram