1 Features

- Consists of 1 Clock lane and up to 4 Data lanes
- Supports MIPI Standard 1.2 for D-PHY
- Supports both high speed and low-power modes
- 80 Mbps to 1.2Gbps data rate in high speed mode
- 10 Mbps data rate in low-power mode
- High Speed Serializer included
- Low power dissipation

2 General Description

The MXL-DPHY-CSI2-TX is a high-frequency low-power, low-cost, source-synchronous, Physical Layer supporting the MIPI Alliance Standard for D-PHY. The IP is configured as a MIPI master optimized for camera interface applications (CSI-2).

The High-Speed signals have a low voltage swing, while Low-Power signals have large swing. High-Speed functions are used for High-Speed data traffic while low power functions are mostly used for control.

3 Block Diagram

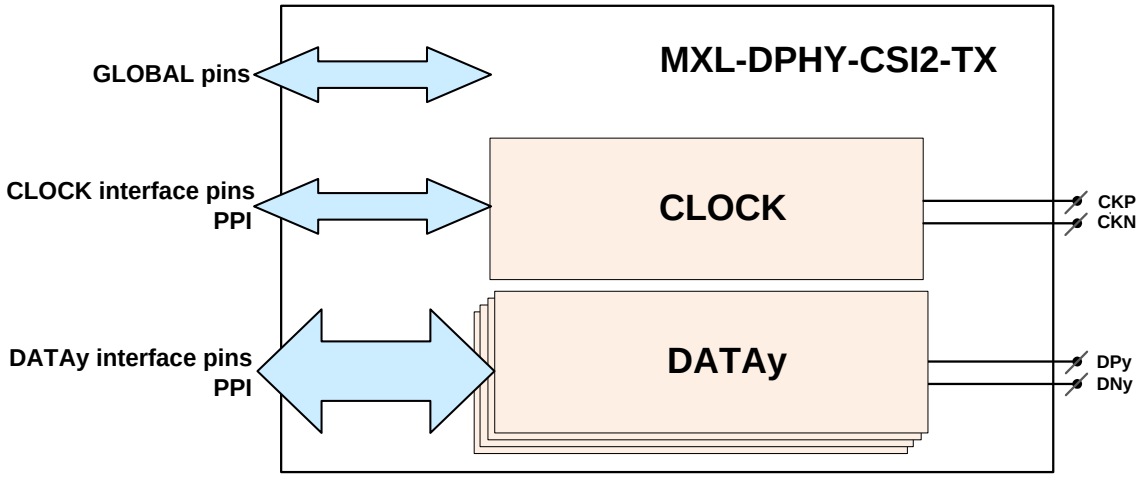

Figure 1: MIPI D-PHY CSI-2-TX Block Diagram

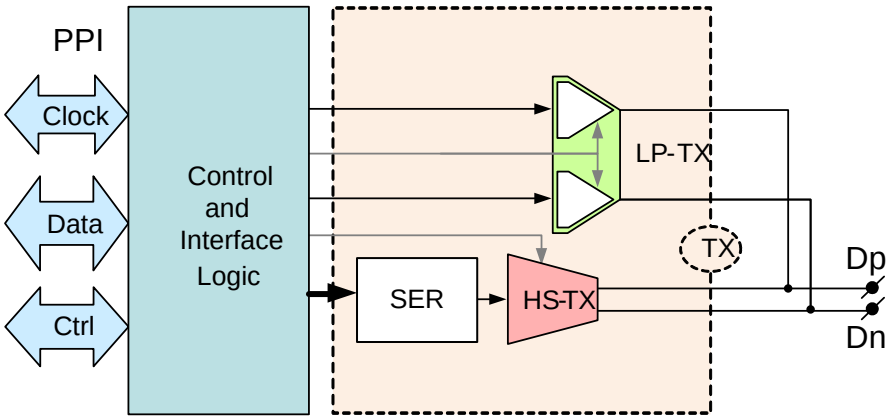

Figure 2: CSI-2 TX Lane Overview

Figure 1 shows the top-level block diagram of the MXL-DPHY-CSI2-TX IP. It consists of a Clock Lane Module and up to four Data Lane Modules. Each of these PHY Lane Modules communicates through a differential line to a complementary PHY at the other side of the lane interconnect. MXL-DPHY-CSI2-TX is partitioned into a Digital Module - CIL (Control and Interface Logic) and a Mixed Signal Module. The D-PHY system is provided as a combination of Soft IP views (RTL, and STA Constraints) for Digital Module, and Hard IP views (GDSII/CDL/LEF/LIB) for the Mixed Signal Module. This unique offering of Soft and Hard IP permits architectural design flexibility and seamless implementation in customer-specific design flow.

The CIL module interfaces with the Protocol and determines the global operation of the Lane Module. The interface between the D-PHY and the protocol is called the PHY-Protocol Interface (PPI).

The Mixed Signal Module includes High-Speed signaling mode for fast-data traffic and Low-Power signaling mode for control purposes. The block diagram of the CSI-2 TX Data lane is shown in Figure 2: DATAy are unidirectional lanes and consist of High-Speed Transmitter (HS-TX), Low-Power Transmitter (LP-TX), and Serializer (SER). CLOCK lane is a unidirectional lane and consists of High-Speed Transmitter (HS-TX), and Low-Power Transmitter (LP-TX).

During normal operation, a Lane switches between Low-Power and High-Speed mode. The change of operating mode requires enabling and disabling of certain electrical functions. These enable and disable events do not cause glitches on the Lines that would result in a detection of an incorrect signal level. Therefore, all mode changes are smooth to always ensure a proper detection of the Line signals.