1 Features

- Compatible with TIA/EIA-644 LVDS Standard
- 49 Mbps - 770 Mbps bandwidth/channel
- Up to 3.08 Gbps data throughput
- 7-bit serial data transmitted per pixel clock per channel
- 4 data channels and 1 clock channel
- Configurable extension to 8 data channels to support Dual Pixel mode
- PLL requires no external components
- Analog, Digital DFT and Loopback testability support

2 General Description

The MXL-LVDS-SR-TX+ is a high performance 4-channel LVDS transmitter implemented using digital CMOS technology. With a maximum transmit clock frequency of 110 MHz, it converts 28 bits of CMOS data into four LVDS data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. The circuit is designed in a modular fashion and desensitized to process variations resulting in a robust design.

3 Block Diagram

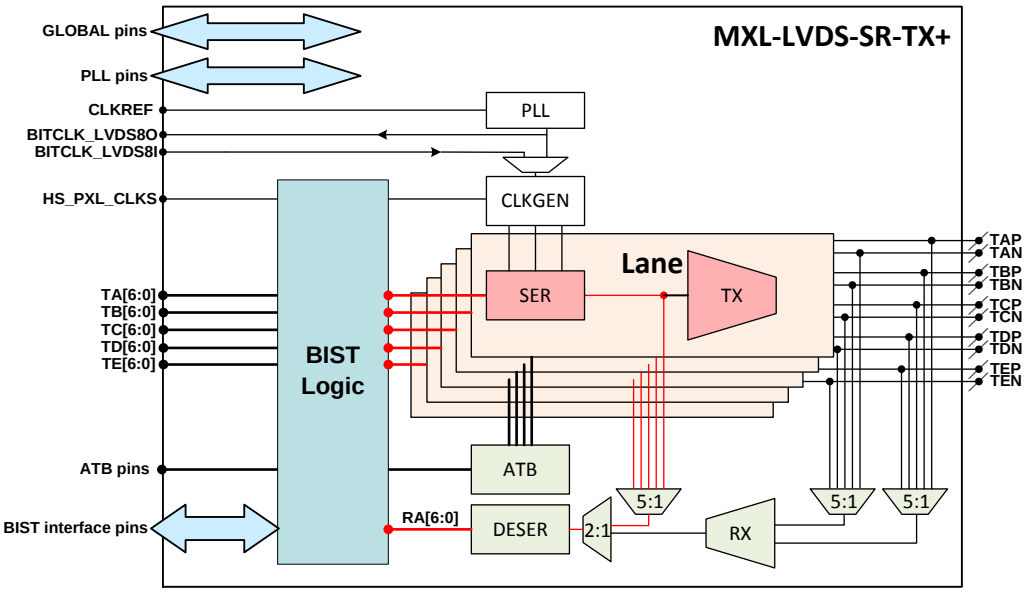

Figure 1: LVDS SR TX Block Diagram