Features:

- Consists of 1 Clock lane and 4 Data lanes
- Complies with MIPI Standard 1.1 for D-PHY
- Supports both high speed and low-power modes
- 80 Mbps to 1.0/1.5Gbps data rate in high speed mode
- 10 Mbps data rate in low-power mode
- High Speed Serializer included
- Low power dissipation

General Description:

The MXL-PHY-CSI2-TX is a high-frequency low-power, low-cost, source-synchronous, Physical Layer compliant with the MIPI Alliance Standard for D-PHY.
The IP is configured as a MIPI master and consists of 5 lanes: 1 Clock lane and 4 data lanes, which make it suitable for camera interface applications (CSI2).
The High-Speed signals have a low voltage swing, while Low-Power signals have large swing. High-Speed functions are used for High-Speed Data traffic while low power functions are mostly used for control.

Block Diagram:

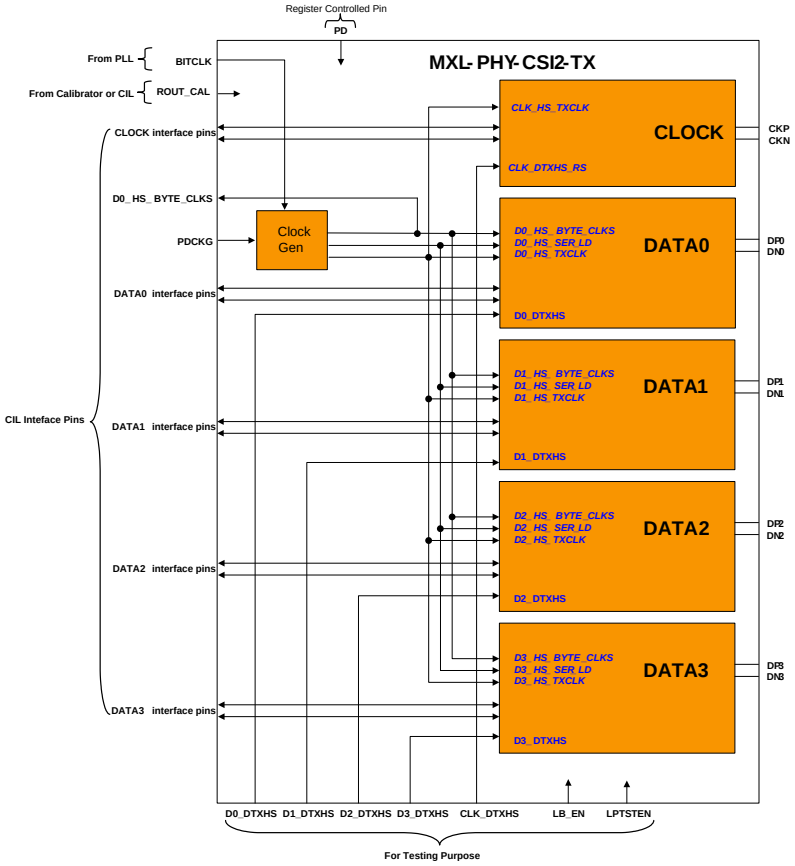

Figure 1 – PHY Block Diagram

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