1 Features

- Consists of 1 Clock lane and up to 4 Data lanes
- Supports MIPI® Alliance Specification for D-PHY℠ Version 1.1
- Supports both high speed and low-power modes
- 80 Mbps to 1.5 Gbps data rate in high speed mode
- 10 Mbps data rate in low-power mode
- High Speed Deserializers included
- Low power dissipation
- Testability support
- Optional resistance termination calibrator

2 General Description

The MXL-DPHY-CSI2-RX is a high-frequency low-power, low-cost, source-synchronous, Physical Layer supporting the MIPI Alliance Specification for D-PHY v1.1.
The IP is configured as a MIPI Slave optimized for CSI-2℠ (Camera Serial Interface) applications.
The High-Speed signals have a low voltage swing, while Low-Power signals have large swing. High-Speed functions are used for High-Speed data traffic while low power functions are mostly used for control.

3 Block Diagram

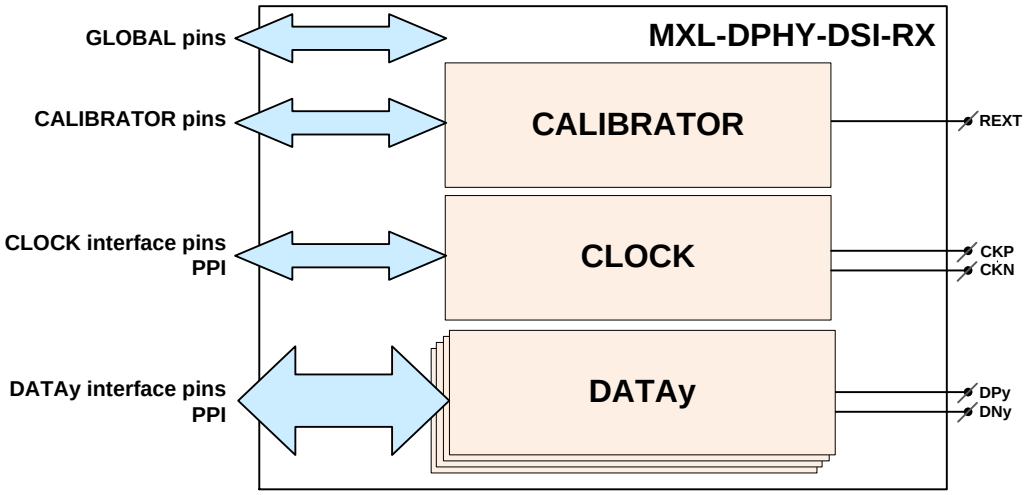

Figure 1: MIPI D-PHY Block Diagram

Figure 1 shows the top-level block diagram of the MXL-DPHY-CSI2-RX IP. It consists of a Clock Lane Module and up to four Data Lane Modules. In addition to the lanes, the IP includes an optional calibrator module for calibration of termination resistance. Each of these PHY Lane Modules communicates through a differential line to a complementary PHY at the other side of the lane interconnect. MXL-DPHY-CSI2-RX is partitioned into a Digital Module - CIL (Control and Interface Logic) and a Mixed Signal Module. The D-PHY system is provided as a combination of Soft IP views (RTL, and STA Constraints) for Digital Module, and Hard IP views (GDSII/CDL/LEF/LIB) for the Mixed Signal Module. This unique offering of Soft and Hard IP permits architectural design flexibility and seamless implementation in customer-specific design flow.

The CIL module interfaces with the Protocol and determines the global operation of the Lane Module. The interface between the D-PHY and the protocol is called the PHY-Protocol Interface (PPI).