Features:

- 25-165 MHz clock support
- Up to 1250 Mbps bandwidth/channel
- Up to 5.0 Gbps data throughput
- Low power CMOS design
- LVDS for low EMI
- PLL requires no external components
- Core Voltage & 1.8V dual power supply
- Optional transmit pre-emphasis
- 10 bit serial data transmitted per pixel clock per channel
- Rising/falling edge data strobe
- Compatible with TIA/EIA-644 LVDS Standard

General Description:

The 28FDSOI-LVDS-4CH-TX-1250-PLL is a high performance 4-channel LVDS Serializer implemented using digital CMOS technology. Both the serial and parallel data are organized into four channels. The parallel data is 10-bits wide per channel. The input clock is 25MHz to 165MHz. The Serializer is highly integrated and requires no external components. It employs optional pre-emphasis to enable transmission over a longer distance while achieving low BER. The circuit is designed in a modular fashion and desensitized to process variations. This facilitates process migration, and results in a robust design.

Block Diagram:

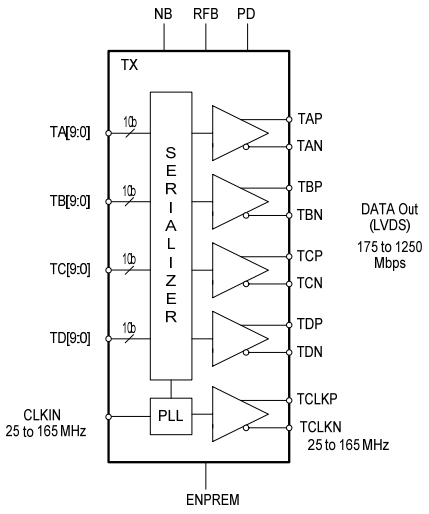

Figure 1 - LVDS 4-Channel Serializer block diagram