

Mixel's MIPI C-PHY/D-PHY Combo IP is Silicon-Proven in Multiple Nodes

The IP is silicon-proven in 40nm and 55nm process nodes, available in 28nm, and is going into high-volume production

San Jose, CA – October 17th, 2017 - [Mixel](#)[®], the leader in mobile mixed-signal intellectual property (IP), announced today that its [MIPI[®] C-PHYSM/MIPI D-PHYSM](#) combo IP is silicon-proven in both 40nm and 55nm process nodes and is going into high-volume production in its customer's products. The IP is also available in 28nm. The MIPI C-PHY/MIPI D-PHY combo supports the MIPI Camera Serial Interface (CSISM) and MIPI Display Serial Interface (DSISM).

Mixel's MIPI C-PHY/MIPI D-PHY combo IP is a high-frequency, low-power, low-cost, physical layer. The PHY can be configured as a MIPI master or MIPI slave, supporting camera interface MIPI CSI-2SM v1.2 and display interface MIPI DSI v1.3 applications in the MIPI D-PHY mode. It also supports camera interface MIPI CSI-2 v1.3 and display interface MIPI DSI-2SM v1.0 applications in the MIPI C-PHY mode. The high-speed signals have a low voltage swing, while low-power signals have large swing. High-speed functions are used for high-speed data traffic, while low power functions are mostly used for control.

Compared to the [MIPI D-PHY](#), the MIPI C-PHY supports data rates 2.28 higher at the same transition rate. This, together with the MIPI C-PHY's embedded clock, results in lower power at higher data rates, and potentially allows for the use of fewer interface pins. The MIPI C-PHY also enables each lane, consisting of a trio, to operate totally independent of the other lanes, making each lane easily assigned to a different link. By embedding the clock, the MIPI C-PHY eliminates the frequency interference caused by the MIPI D-PHY clock lane.

The combo IP not only shares the serial interface pins, but Mixel's implementation also reuses all the MIPI D-PHY functional blocks for the MIPI C-PHY, minimizing area and leakage power.

"We see a lot of traction with this combo IP, which has been designed into several Mixel customers' SOCs," said Ashraf Takla, Mixel's President and CEO. "Clearly, supporting MIPI D-PHY, the most widely adopted MIPI PHY today, while enabling the transition into higher data rate, next-generation products supporting MIPI, is a very powerful proposition."

The advantages that the MIPI C-PHY offers come at the expense of additional complexity, such as unique clock and recovery, which is programmable based on data rate. The MIPI C-PHY has seen wide adoption in camera applications, and display providers have also started supporting the MIPI C-PHY in some of their offerings.

Mixel will be co-presenting a technical presentation with Qualcomm Technologies, Inc. titled, “MIPI C-PHY/D-PHY Dual Mode Subsystem Performance & Use Cases” and will be demonstrating many of its own and its customers’ products at [MIPI DevCon 2017](#), October 27, 2017, in [Bangalore, India](#), and October 31, 2017, in [Hsinchu City, Taiwan](#).

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About Mixel:

Mixel is the leader in mixed-signal mobile IPs and offers a wide portfolio of high-performance mixed-signal connectivity IP solutions. Mixel’s mixed-signal portfolio includes [PHYs and SerDes](#), such as Mobile PHYs ([MIPI[®] D-PHYSM](#), [M-PHY[®]](#), [C-PHYSM](#) and [LVDS](#)), and high-performance PLL and DLL IP cores. For more information contact Mixel at info@mixel.com or visit www.mixel.com.

About the MIPI Alliance:

MIPI (MIPI[®]) Alliance is a global, collaborative organization comprised of companies spanning the mobile ecosystem that are committed to defining and promoting interface specifications for mobile devices. MIPI Specifications establish standards for hardware and software interfaces which drive new technology and enable faster deployment of new features and services across the mobile ecosystem. For more information, go to www.mipi.org.

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