TSMC OIP 2019

Silicon Accurate Analog Mixed Signal Verification of Mixel's Dual Mode C-PHY/D-PHY IP for AR/VR Display ICs with Mentor AFS
Agenda

- Mixel Overview
- VR AR MR Industry trends
- XR Display System
- Mixel C-PHY/D-PHY IP
- Design & Verification Challenges
- Analog FastSPICE (AFS) Platform
- Simulation and Silicon Results
- Summary
Mixel Overview

- Leading provider of mixed-signal IP since 1998
- Industry leader in MIPI® interfaces and contributing member of the MIPI Alliance since 2006
- First IP provider to demonstrate silicon-proven D-PHY℠, C-PHY℠, and M-PHY®

Customer-centric focus:
- We customize our IPs to help differentiate our customers’ products
- Our methodology has been optimized to achieve first-time silicon success, no exception
- We consistently go the extra-mile for our customers
Mixel IP Portfolio

- Mixed-signal IP provider with emphasis on PHY
  - MIPI PHY: D-PHY, C-PHY, M-PHY
  - LVDS SerDes
  - Multi-standard SerDes: C/D-PHY, LVDS/D-PHY

- Complete integrated solution includes PHY, controller, and platform

- Widest support of optimized PHY configurations using patented topologies

- Support ALL MIPI HS PHYs

- Widest coverage of process nodes and foundries: silicon-proven in 9 different nodes and 8 different foundries
Mixel MIPI PHY Customers

And many others that cannot be disclosed at this time.
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What is XR

- Virtual Reality (VR)
  — Fully artificial environment

- Augmented Reality (AR)
  — Virtual objects overlaid on real-world environment

- Mixed Reality (MR)
  — Virtual environment combined with real world

Source: Pinterest, AR VR application pin
VR AR MR Industry trends

- AR and VR increasingly enhanced with AI
  - Computer vision allows computers to understand what they are “seeing” through cameras resulting in smart applications and use cases

- VR and AR is increasingly used in training and teaching
  - Virtual environments allow students to practice anything from construction to flight to surgery without the risks associated with real-world training
  - Example: HoloLens technology is used in military training

Source: Pinterest, AR VR application pin
VR AR Industry trends

- **Consumer Entertainment VR hits the mainstream**
  - More realistic and accurate simulations of our real world resulting in more immersive entertainment experiences

- **VR and AR environments becoming increasingly collaborative and social**
  - Virtual “conference calls” where participants can see and interact with each other, or socializing and relaxing with friends is soon becoming a reality

- **AR increasingly finding its way into vehicles**
  - Powered by AI in-vehicle AR has the potential to improve safety and increase comfort and driver convenience
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XR Display System

- Video over DP or USB-C connector from PC or smartphone
XR Displays Drive Video Interface Technology

- Higher PPI eliminates “screen door” effect & enables ability to read text
  - Resolution: 2Kx2K minimum, better = 3Kx3K, ideal = 4Kx4K

- AMOLED, LCOS, and OLEDoS: Leading Near-Eye Screen Technologies
  - The response time of AMOLED is lower than that of liquid crystal by an order of magnitude, avoiding streaking and blurring due to VR interaction

- VR systems require higher video bandwidths to match display resolutions
  - Need 32Gbps raw bandwidth GPU to display
  - Need DP DSC support to exceed dual 5.5M pixel displays and MIPI DSC support to exceed 6.2M pixel displays
  - Need SPR support for optimized OLED bandwidth
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Mixel C-PHY/D-PHY IP integrated in DDIC

- **Combo PHY can be configured as either a C-PHY or D-PHY**
  - Configurable for transmit (TX) and receive (RX), additional optimized configurations for TX and RX provide smaller area and higher performance
  - Supports lane swapping and pin swapping features

- **MIPi D-PHY mode supports**
  - MIPI Master or Slave
  - Display interface DSI v1.3 and Camera interface CSI-2 v1.2
  - 2.5 Gbps data rate per lane with De-skew calibration
  - BIST with 100% coverage for HM
  - 4 lanes in D-PHY (10 pins)

- **MIPi C-PHY mode supports**
  - Display interface DSI-C v1.0 and Camera interface CSI-2 v1.3
  - 80 Msps to 2.5 Gsps symbol rate per lane in high speed mode
  - T1 and T2 modes
  - BIST with 100% coverage for HM
  - 3 lanes in C-PHY (9 pins)
Why dual-mode C-PHY/D-PHY interface is required

- **Minimal Overhead**
  - Sharing of the serial interface pins
  - All D-PHY blocks are re-used for C-PHY

- **Enhanced PPA**
  - Flexibility to support both PHY
    - C-PHY @ 2.5 Gsps (≈5.7 Gbps)
    - D-PHY @ 2.5 Gbps
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XR System Challenges

- **High Bandwidth Requirements**
  - High display resolution
  - Faster frame rate
  - Higher sensor resolution
  - High dynamic range

- **SOC Design Constraints**
  - Low Power / Heat
  - Package / Minimal pin count
  - Minimize die area – Support multiple use cases

Source: Qualcomm Extended Reality
Custom IP Verification Challenges

- Traditional SPICE simulators do not have performance and capacity
- Need nanometer SPICE accuracy to validate key specifications
- Need tighter tolerances to increase the dynamic range (>100dB)
- Need to include layout parasitics and device noise
- Long runs for verification and characterization

<table>
<thead>
<tr>
<th>MIPI D-PHY/C-PHY TX</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Critical Specs/ Design Targets</td>
<td></td>
</tr>
<tr>
<td>Data Rate per lane</td>
<td>2.5Gbps for D-PHY mode</td>
</tr>
<tr>
<td></td>
<td>5.7Gbps for C-PHY mode</td>
</tr>
<tr>
<td>Power efficiency Target</td>
<td>&lt;3-4mW/Gbps</td>
</tr>
<tr>
<td>TX Jitter</td>
<td>0.3 UI</td>
</tr>
<tr>
<td>CLK to Data skew</td>
<td>0.2 UI</td>
</tr>
<tr>
<td>HS TX diff swing</td>
<td>140-270mV</td>
</tr>
<tr>
<td>HS TX common mode voltage</td>
<td>150-250mV</td>
</tr>
</tbody>
</table>
SoC Verification Challenges in nm Technologies

- Increasing Parasitics
- Increasing Variability
- Increasing Resistance
- Increasing Device Noise
- New Aging Requirements
- Exponential Delay Variation

Quite complex! Quite expensive!
Challenges to Matching Silicon

**Simulation**
- Model accuracy (SPICE, Variation, Corners, S-Parameters)
- Process variation (global & local)
- Circuit simulator accuracy (noise floor)
- Layout and Thermal effects
- Distribution uncertainty due to sample size
- Parastastics (extraction, variation)
- Aging effects
- Device noise, noise bandwidth, runtime
- Measurement post-processing
- System level modeling

**Silicon**
- Specific silicon manufacturing
- Lot, wafer, die selection
- Specific contextual circuit activity
- Test equipment, method, resolution...
- Probe effects & variability
- Temperature & variation
- Voltage & variation
- Distribution uncertainty due to sample size
- Measurements
- Measurement post-processing
- Compliance testing

*Simulated Circuit* → *Uncertainty* → *Measured Silicon*
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Analog FastSPICE (AFS) – nm Circuit Verification

<table>
<thead>
<tr>
<th>The Problem- Simulation Accuracy, Performance &amp; Capacity</th>
<th>AFS Industry-Proven Leadership</th>
<th>The Value- Faster TTM and Lower Risk</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Accuracy vs Silicon</td>
<td>• Industry leader for nanometer circuit verification</td>
<td>• Foundry certified down to 5nm</td>
</tr>
<tr>
<td>• Complex models for FinFET</td>
<td>• &gt;175 customers worldwide</td>
<td>• &gt;2x faster vs parallel SPICE simulators</td>
</tr>
<tr>
<td>• Need advanced analyses</td>
<td>• Foundry certified by the world’s leading foundries</td>
<td>• &gt;20M-element capacity</td>
</tr>
<tr>
<td>• Need to include additional effects</td>
<td>• Drop-in compatibility in existing flows</td>
<td>• Signoff Accuracy for nm designs</td>
</tr>
<tr>
<td>• Device noise</td>
<td></td>
<td>• Must have for PLL, ADC/DAC, High-Speed I/O</td>
</tr>
<tr>
<td>• Layout parasitics</td>
<td></td>
<td>• Proven to be within 1–2 dB of silicon</td>
</tr>
<tr>
<td>• Circuit verification bottleneck</td>
<td></td>
<td></td>
</tr>
<tr>
<td>• Longer simulation times</td>
<td></td>
<td></td>
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<tr>
<td>• Need many more simulations</td>
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- Device Noise vs Process Node/Supply Voltage

Silicon accurate SerDes Verification
AFS and PLL Verification Challenges

- **Performance**
  - 2x-6x faster transient simulations*
  - 4x-5x faster transient noise simulations* (jitter, phase noise)
  - Near Linear Scaling - Monte Carlo (using MCP/DMCP)
  - Near Linear Scaling - Corners (using MCP/DMCP)
  - 5x-10x faster PNOISE for switched cap circuits*

- **Accuracy**
  - Foundry certified down to 5nm (including aging)
  - Silicon accurate Jitter and Phase Noise (1-2 dB)
  - Nm SPICE accuracy for higher data rates
  - Nm SPICE accurate power measurements
  - Accurate S-parameter analysis

- **Capacity**
  - > 20 M element capacity for AC/DC/Transient
  - > 1 M element capacity for PSS/PNOISE

* versus parallel SPICE simulators
TSMC Custom Design Reference Flow

**AFS Platform Full-Spectrum Device Noise Analysis**

- Problem: Device noise in analog, mixed-signal, and RF circuits limits performance at 45nm and below
- Solution: Use device noise analysis to characterize performance of analog, mixed-signal, and RF circuits
- Technology: AFS Platform Full-Spectrum Device Noise Analysis for transient noise and periodic noise
- Benefit: Verify PLLs, ADCs, SerDes, and other circuits with nm SPICE accuracy including all device noise effects
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Silicon Measurement/Simulation Correlations for D-PHY mode

The eye diagram is courtesy of Synaptics

From AFS Simulation
Silicon Measurement/Simulation Correlations for D-PHY mode

<table>
<thead>
<tr>
<th></th>
<th>Silicon Measurement</th>
<th>AFS Simulation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Eye Height</td>
<td>293mV</td>
<td>285mV</td>
</tr>
<tr>
<td>Eye Width</td>
<td>377ps</td>
<td>380ps</td>
</tr>
</tbody>
</table>

AFS Simulation Results Correlation with Silicon Measurements is within **0.8% - 2%**

Mentor AFS is certified for latest TSMC 5nm FinFET process
Mixel MIPI C-PHY℠ Eye Diagram at 2.5Gsp/s

The eye diagram is courtesy of Synaptics
PLL Simulation Results
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Summary

- Growing applications of Virtual and Augmented reality devices demands high bandwidth, high resolution and low power specifications for VR/AR ICs
- Mixel is industry leader in MIPI interface PHYs and demonstrated silicon-proven D-PHY℠, C-PHY℠, and M-PHY® with TSMC
- Mentor’s AFS is essential for Mixel's Dual Mode C-PHY/D-PHY IP Design & Verification
  
  Performance characterized with AFS Platform enabling
  ✓ Rapid and accurate block-level and top-level analysis
  ✓ Good simulation-to-silicon correlation within 0.8% - 2%
- TSMC Models predict measured behavior with good confidence