Mixed-Signal Excellence

MIPI D-PHY RX+: An Optimized Test Configuration

About the Authors

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D-PHY℠ RX+ is a Mixel proprietary implementation[1] for Camera Serial Interface (CSI) and Display Serial Interface (DSI) D-PHY Receiver optimized for small area and low power, while achieving full-speed production testing, in-system testing, and higher performance compared to traditional receiver configurations.

There are multiple reasons why it is crucial to test an IC as early as possible in its life cycle such as cost and safety concerns. The Rule of Ten, which is widely accepted in the electronics industry, states that the cost of discovering a defective chip increases by an order of magnitude at each successive level of integration, from die/package, to board and system.

In safety sensitive applications, cost and risk grow even faster, and the implications of a failing part are intolerable. As electronic component contents rapidly grows in those applications, the cost of failure increases substantially, and detection of any degradation in performance as early as possible is highly desirable. Full-speed production testing enables detection of manufacturing faults and helps drive down the number of defects to zero, as required in safety sensitive applications such as in the automotive industry.

Testing of integrated circuits is done in order to achieve one of three goals: detection, diagnosis, and device characterization. Detection determines whether or not the device under test has any faults. This involves identification of process flaws as well as detection of chips that must not be sold to customers. Diagnosis involves locating and identifying of a specific faults that are present in the tested device. Device characterization is the identification of errors in the actual design or in the testing procedure.

MIPI Physical layer differs significantly from many existing interfaces. In particular the D-PHY can and does switch in real-time between two modes, High-speed (HS) using LVDS signals and Low-power (LP) using single-ended CMOS logic signals. It is difficult to test both HS and LP blocks using ATE. That is why BIST is a valuable feature particularly for D-PHY testing.

BIST has many benefits including the ability to test the chips across several layers of abstraction (IC, PCB, etc.), improving controllability and observability, external test equipment is simplified or eliminated, tests are performed at chip speed (which is increasingly difficult using ATEs), and BIST performance follows process technology improvements, whereas ATEs technology lags behind.

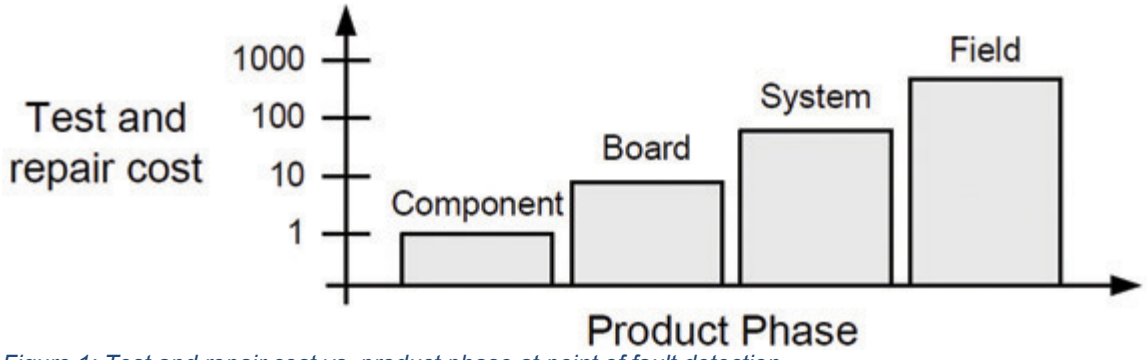

Figure 1: Test and repair cost vs. product phase at point of fault detection

BIST has drawbacks as well. Area overhead can lead to yield deterioration and reliability degradation, additional hardware in the loop causes increased delays and timing issues, and BIST strategy must be decided early in the development cycle so it can be implemented on-chip.

The D-PHY universal Lane, shown in Figure 2, has many blocks connected to the high-speed serial interface (LPTX, HSTX, LPRX, HSRX, LP-CD) resulting in high parasitic cap, not only due to block input capacitance but also due to parasitic interconnect capacitance. This puts an artificial upper limit on data rate.

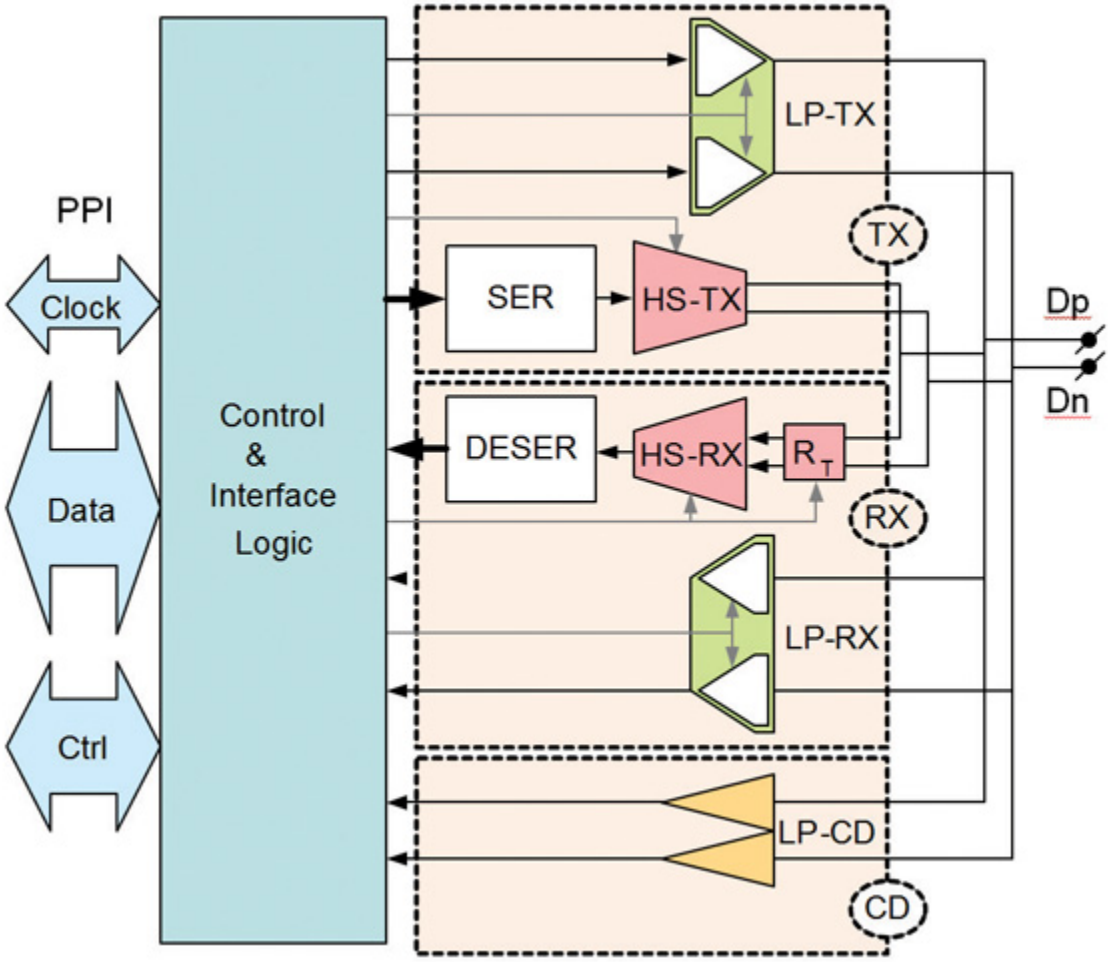

Figure 2: D-PHY Universal Lane configuration supports testability at the expense of large overhead

Traditional D-PHY implementation that can support at-speed production test uses the Universal Lane configuration. A D-PHY RX application would require inclusion of both the HS & LP TX in each of the data lanes in addition to the clock lane. This results in a considerable amount of overhead in RX applications, since D-PHY HS and LP TX are significantly larger than the corresponding RX only configuration, which is shown in Figure 3.

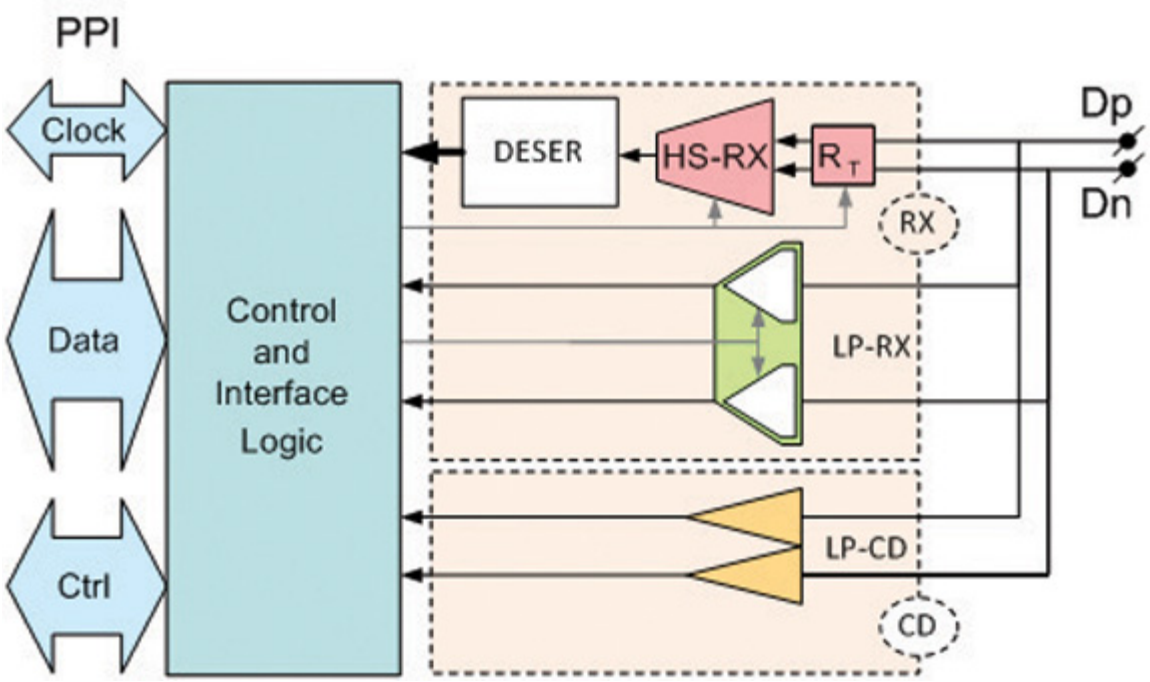

Figure 3: RX only configuration is quite smaller that a Universal lane, but cannot support full-speed production test

The Mixel proprietary implementation of the MIPI D-PHY compliant RX+ configuration combines the small area and improved performance of RX configuration with the testability and diagnostics that are possible with Universal lane configuration, the best of both worlds. This is shown in Figure 4.

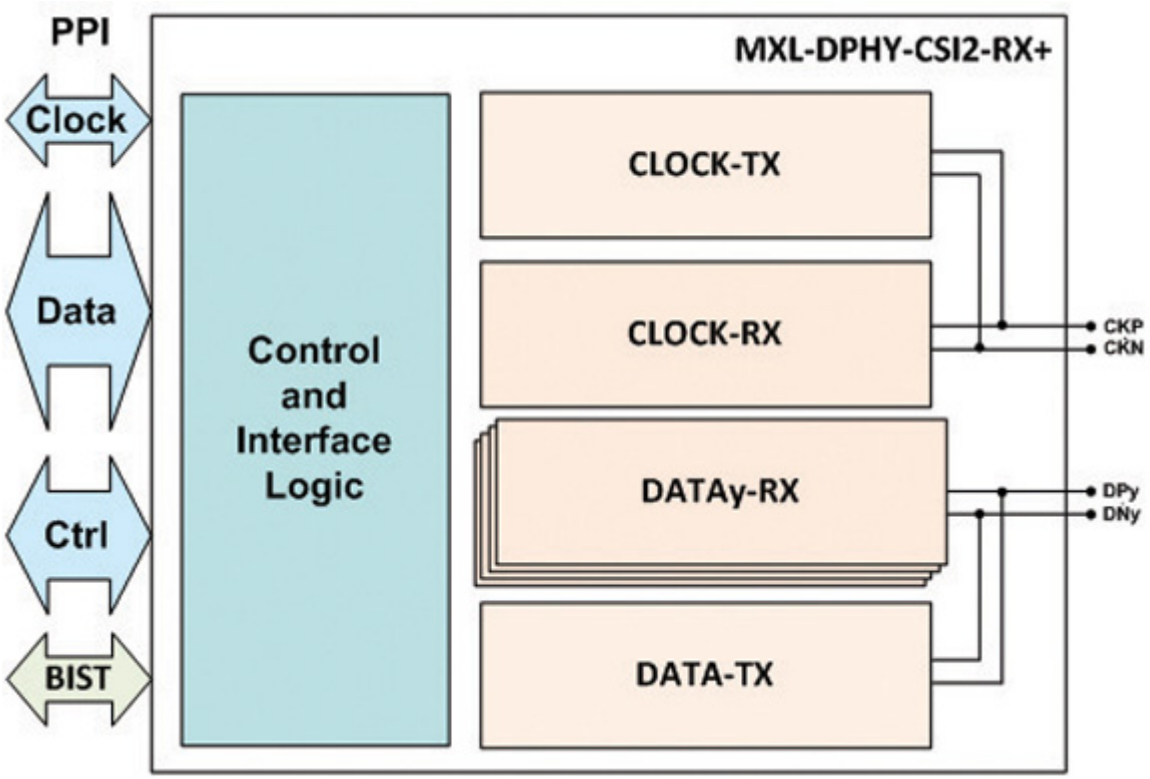

Figure 4: Mixel's RX+ optimized configuration

Since the D-PHY TX area is significantly larger than that of RX, Mixel's RX+ configuration has smaller area and standby current, as only two transmitters are need instead of the five transmitters that would be needed for a conventional 4 data-lanes Universal lane configuration. The reduction in area is about 35% while standby power reduction is about 50%.

The RX+ configuration has clear advantage in many aspects. Mixel proprietary implementation of RX+ configuration enables early detection and diagnosis of faults through the whole life cycle of the product from wafer-sort all the way to in-system testability. It also simplifies ATE requirements, and enables at-speed testing (production and in-system), with minimal increase in area.

To summarize, the RX+ is a Mixel innovative solution to D-PHY's serious testability challenges. This unique MIPI compliant configuration results in area and power savings and improved testability in full-speed production test and in in-system testability and diagnostics. It combines the testability of universal lane with the small size and improved performance of RX only configuration.

For information about Mixel's IP portfolio, visit mixel.com/ip-cores.

