Mixed-Signal Excellence

Dual Mode C-PHY/D-PHY: Enabling Next Generation of VR Displays

About the Authors

Ashraf Takla, *Mixel, Inc., CEO*

Cedric Bertholom, *ST-Ericsson, CTO*

The MIPI Alliance was created in 2003 to benefit the entire mobile industry by establishing standards for hardware and software interfaces in mobile devices.

One critical component of any mobile device is the Physical layer (PHY). The first PHY specification that the MIPI Alliance released in 2009 was the D-PHY. The D-PHY currently operates up to 1Gbps and supports both Camera Serial Interface (CSI-2) and Display Serial Interface (DSI), which are increasingly used in both feature and smart phones.

To enable next generation smart phones and tablets, the MIPI Alliance is releasing the M-PHY®1.0 specification by second quarter of 2011, and plans to release versions 2.0 and 3.0 later in the year to support data rates up to 6Gbps at considerably low power. The M-PHY is the most versatile PHY specification available for adoption today.

Benefits and challenges, two faces of the same coin

With this unprecedented versatility come many benefits as well as many challenges. The M-PHY supports **plesiochronous**[i] as well as **mesochronous**[ii] operations, speeds from 10Kbps up to data rates of 6Gbps while maintaining low power operation, achieving low electro-magnetic-interference (EMI), supporting a variable number of links, sub-links, and data lanes, multiple media options, and a growing number of use-case in traditional and non-traditional mobile applications.

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Flexibility and speed

The M-PHY supports two types of operations. Type-I M-PHY supports plesiochronous operation where the PHY on the two sides of the link can operate at slightly different data rates and mesochronous operation where the PHY on both sides of the link use the same reference clock. Type-II supports mesochronous operation only. The high level block diagrams of the two types are shown in Figure 1. This allows use-cases where the reference clock is available on both sides of the link, such as DigRF, to use a simpler more optimized PHY, while also accommodating other use-cases.

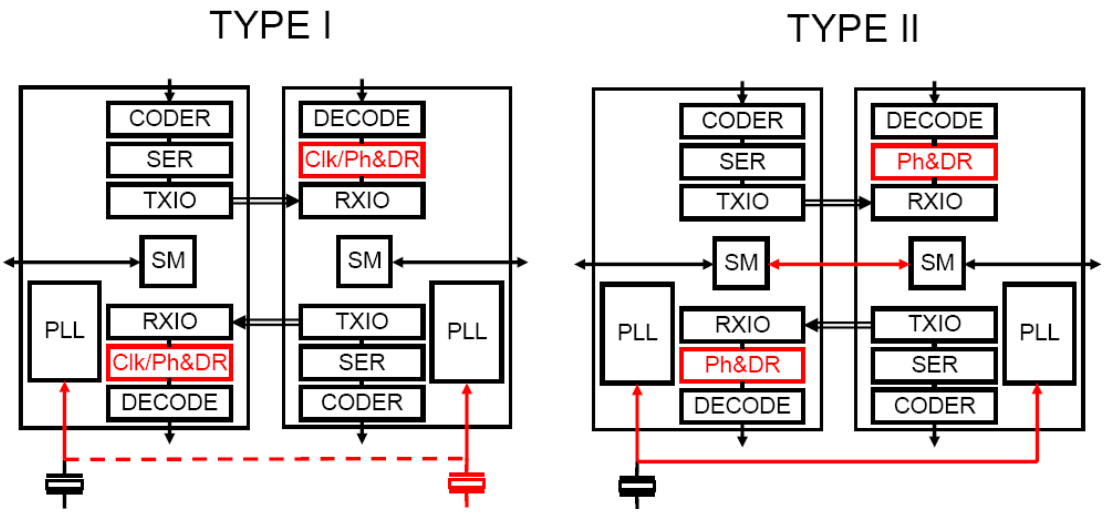

Figure 1: M-PHY Type I and Type II clocking architecture / Source: MIPI Alliance

One of the critical features demonstrating the M-PHY versatility is its ability to operate over a wide data range, as low as 10kbps and as high as 5.8Gbps. Additionally the M-PHY state machine allows dynamic transition over this wide data rate range with minimal overhead. The implementer is then able to use the minimum possible amount of power for any particular task and application. The M-PHY accomplished this by supporting 3 different High-Speed (HS) Gears, 1 through 3 (G1-G3), as shown in Table 1, and multiple Low Speed (LS) options, as shown in Figure 2.

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Gbps	A	B
HS-G1	1.25	1.45
HS-G2	2.5	2.9
HS-G3	5.0	5.8

Table 1: M-PHY supported data rates / Source: MIPI Alliance

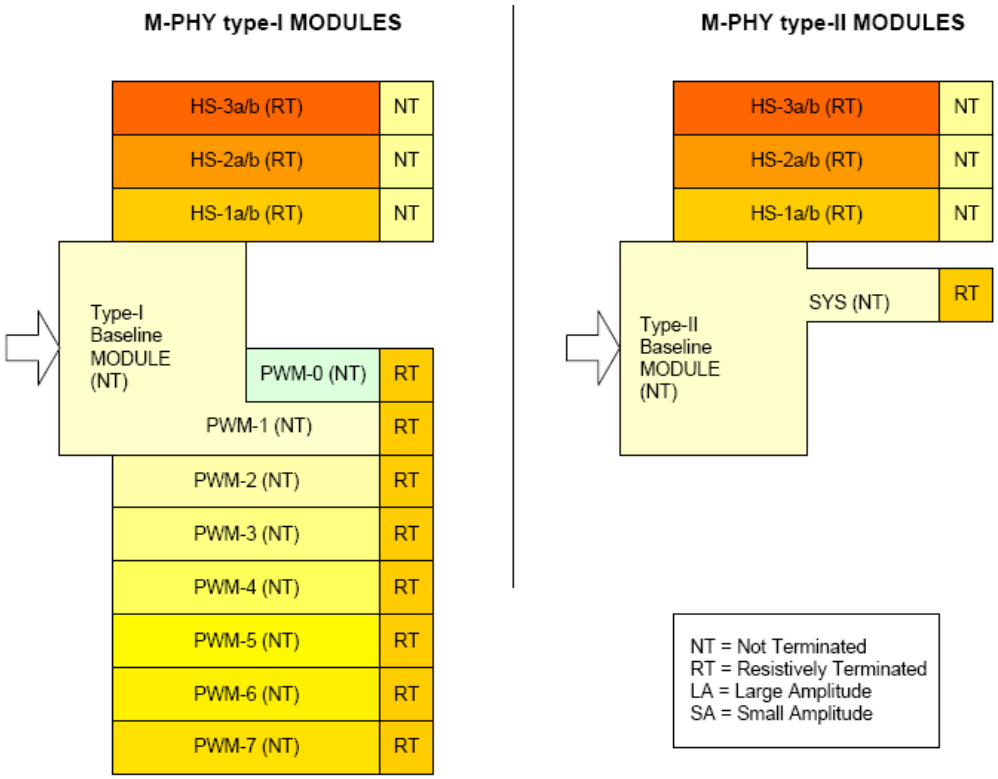

Figure 2: M-PHY Type-I and Type-II Gears / Source: MIPI Alliance

For TYPE-I M-PHY, the specification makes available 8 different LS Gears (G0-G7), starting at 10kbps up to 576Mbp, using Pulse-Width-Modulation (PWM). Since the clock is embedded in PWM data, no Clock/Data Recovery (CDR) or even a PLL is needed in this low-speed, low-power mode of operation. For TYPE-II there is no need to use PWM since the same reference clock is available on both sides of the link and thus a less noisy and simpler LS operation is possible[iii].

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Power

A mobile terminal PHY's real value is largely tied to its ability to be a power miser. In the case of the M-PHY minimizing power is accomplished by:

- Power gradation through multiple states and extensive use of save states, as shown in Figure 3
- Fast and simple transition between all states
- Fast wake up time in LS mode without the need for synchronization or CDR
- Aggressive power targets for both HS and LS operation. See Figure 4
- System is optimized for send and stop strategy, with NOP/Filler use, as shown in Figure 5.

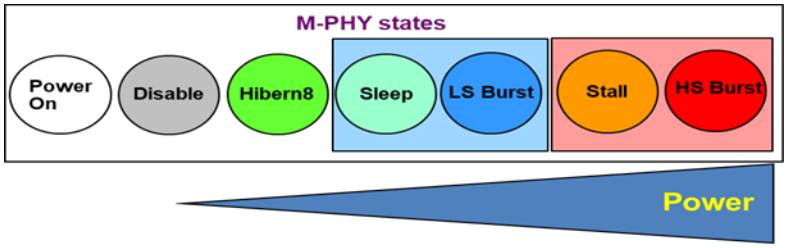

Figure 3: M-PHY states and power grading / Source: STE

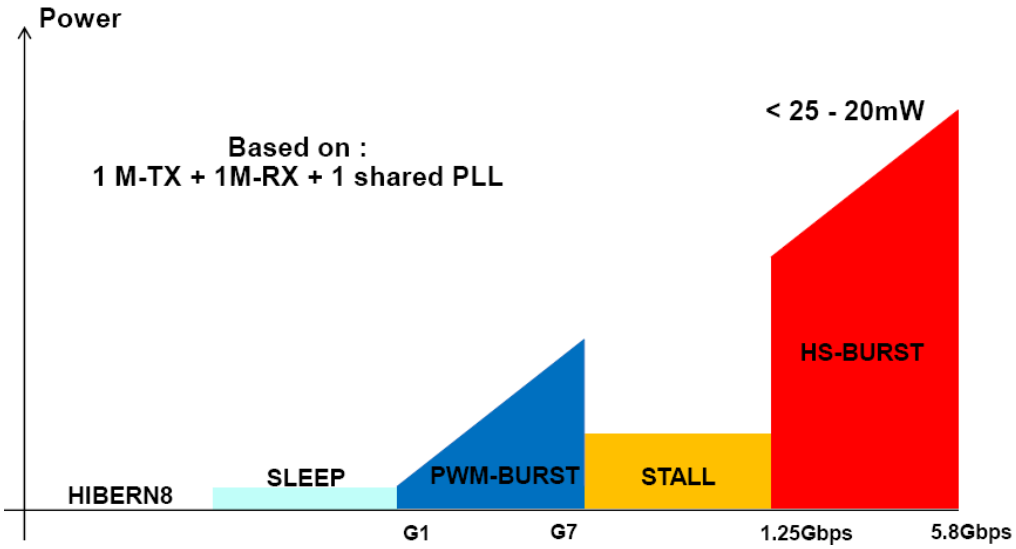

Figure 4: M-PHY aggressive power target for HS and LS operation / Source: STE

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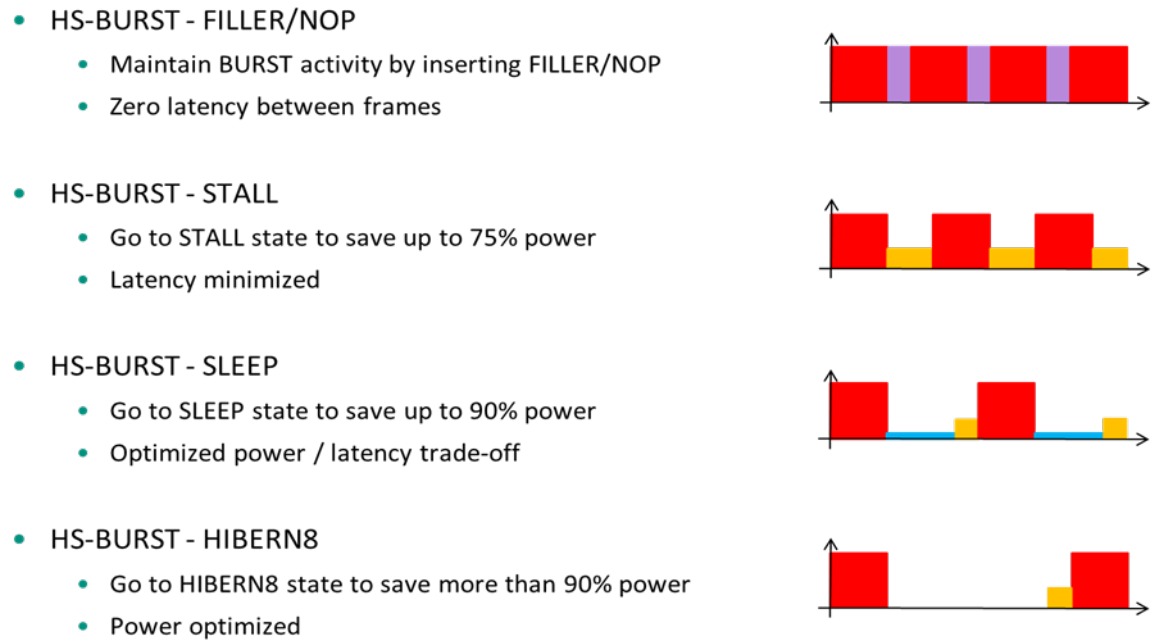

Figure 5: Send & Stop strategies / Source: STE

The M-PHY makes efficient use of many different modes of operations: Unpowered, Disable, Hibernate (Hibern8), Low Speed Mode and High Speed Mode. The state machine is shown in Figure 6 below.

Disable mode is the lowest power mode entered into once the power supply is turned on. Hibern8 is an ultra low power state, which can be used without configuration loss. It enables online wake up capability without any side band signals (in Type-I). The transition to another M-PHY state takes hundreds to thousands of microseconds. That recovery time is programmable to fit the application requirements.

The LS and HS modes each define power saving states, Sleep and Stall respectively in addition to their respective burst states.

LS-Mode is used when the application requires low activity level. Power saving is accomplished since no PLL, CDR, or synchronization is required. This not only saves power but also minimizes transition time, which is typically in the range of microseconds.

HS-Mode targets power numbers in the order of pJ/bit. In this mode, the M-PHY delivers data with an aggressive total power target of 20 mW. Data recovery is required to recognize bit information at Gbps speed. A synchronization sequence locks the receiver CDR phase and frequency in an extremely short time. The M-PHY specification

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does not dictate this sequence length, instead that is determined by the application. This allows each application to configure and use the M-PHY in the most optimal way.

HS-MODE utilizes the power-saving Stall state to reduce the power consumption by stopping lane activity and any unnecessary power dissipation, while offering a fast transition in the range of ns.

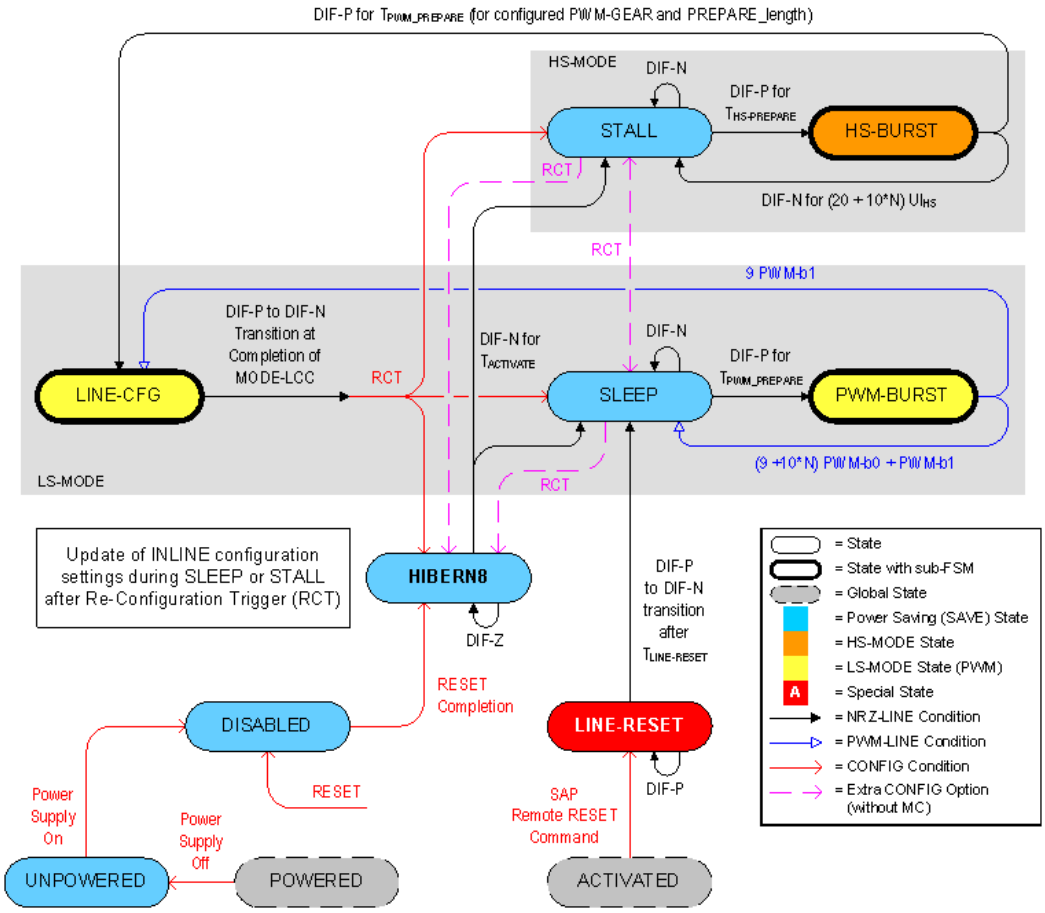

Figure 6: The M-PHY state machine / Source: MIPI Alliance

Programmable amplitude and switchable termination

To save as much power as possible, in addition to the multiple low power modes employed, the M-PHY supports both programmable low amplitude and switchable termination. There are two amplitude settings, Large Amplitude (LA) and Small Amplitude (SA). The M-PHY can also operate terminated, or un-terminated, as shown in Figure 7. For LS operation, SA un-terminated mode can be used to minimize power. HS operation support of terminated operation is mandatory, while support for un-terminated operation is optional.

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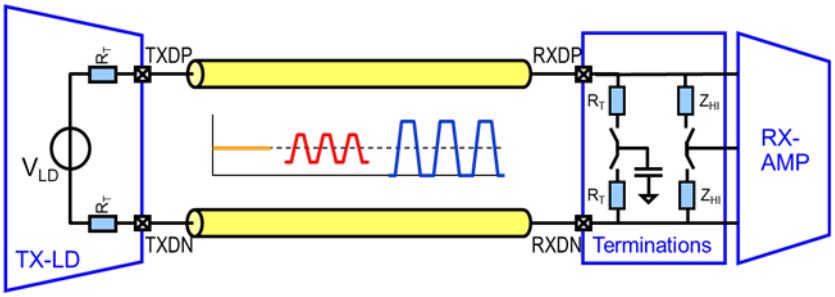

Figure 7: The M-PHY Transceiver example / Source: MIPI Alliance

EMI mitigation

Another critical parameter for operation in a mobile environment is EMI. Minimal EMI is needed to insure proper operation of sensitive RF receivers. To meet this challenge the M-PHY employs many EMI mitigation techniques. They are:

- Dual data rates for each HS Gear: Each of the HS Gears supports two different data rates, A and B, as shown in Table 1. This feature allows moving common mode M-PHY signal away from sensitive RF LNAs signals such as GPS LNA or when handset has to support different geographical regions.
- Programmable slew rate: Implementation specific but always monotonic
- Minimize signal amplitude, by using programmable amplitude
- Limit common-mode noise by using 8b10b coding

All those mitigation strategies results in reduced common mode Power Spectrum Density (PSD) of the driver under -110 to-140 dBm/Hz range, as shown in Figure 8.

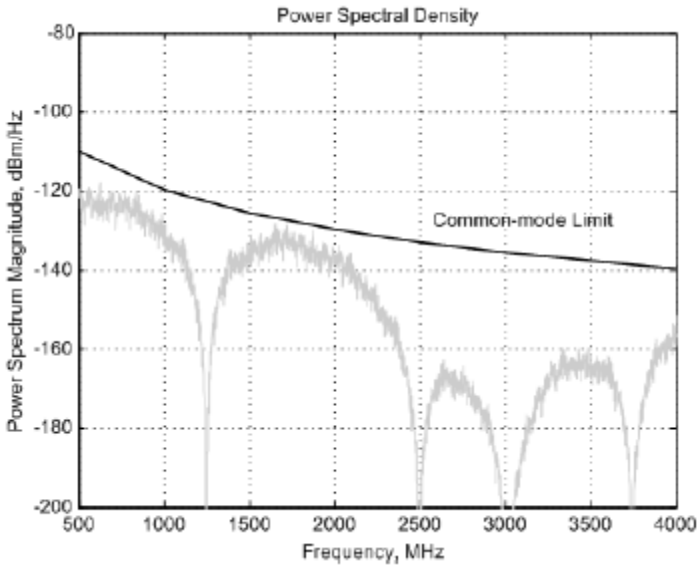

Figure 8: Common mode PSD / Source: MIPI Alliance

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Link variability

To be able to support a wide range of applications and multiple generations of mobile devices, a flexible aggregate BW is required. To meet this challenge, the M-PHY supports a variable number of links, sub-links, and data lanes as shown in Figure 9.

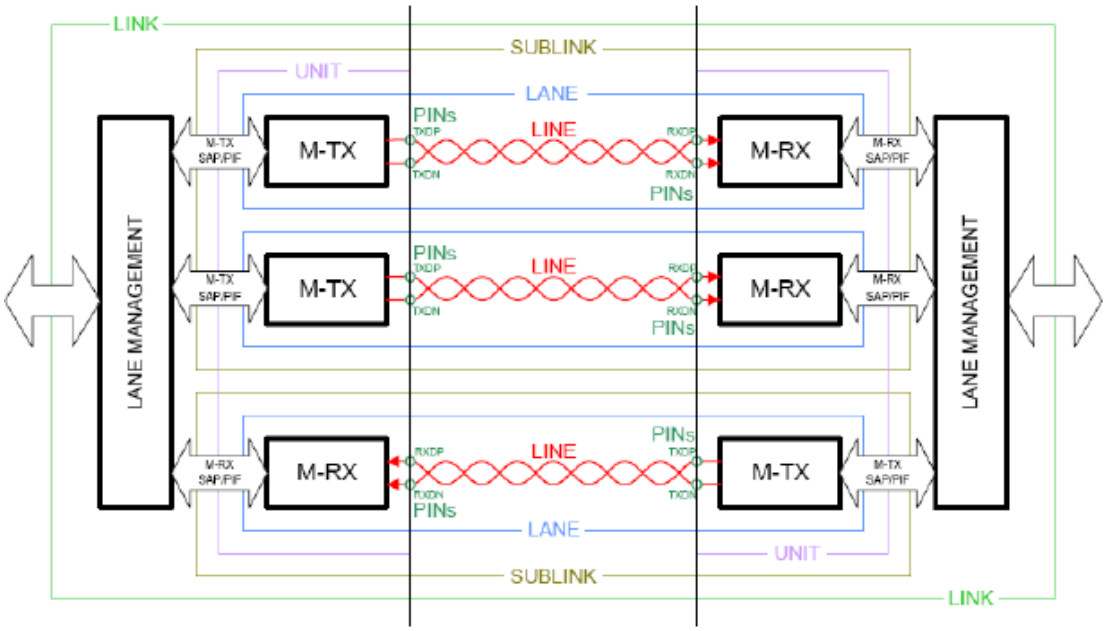

Figure 9: Architecture of the M-PHY LINK, showing sub-links and lanes / Source: MIPI Alliance

A multitude of use-cases, a wide range of bandwidth, and various interconnect media support under one umbrella

This is where M-PHY versatility pays off. Although the initial intent of the MIPI Alliance was to use the M-PHY for traditional mobile applications such as connecting cameras and displays to a host processor, the M-PHY versatility made it an attractive PHY in other applications that were not initially anticipated.

First there was DigRF protocol that is used for chip-to-chip communication between the baseband processor and the RF IC. Next there was the Universal Flash Storage (UFS), which is a JEDEC standard[iv], and then Low-Latency-Interface (LLI) which is also used for chip-to-chip protocol and targets low latency in the magnitude of 80ns. Those different applications use a combination of TYPE I, TYPE II and HS Gears as shown in Table 2[v].

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Application	Type	HS-GEAR
DigRF v4	II	1
CSI-3	I	2
DSI-2	I	2
JC-64.1 UFS	I	2
LLI	I	3

Table 2: Multiple M-PHY use-cases / Source: Mixel

Additionally, the M-PHY specifications support both electric and optical media, by using an optional Optical Media Convertor (OMC), which does not require any dedicated protocol layer. By allowing for an optical option as shown in Figure 10, the M-PHY can extend its reach to longer distances, without consuming excessive power in implementing pre-emphasis or complex equalization schemes, and allow for adoption of complex, multi-axis, mechanical joints, while reducing EMI even further.

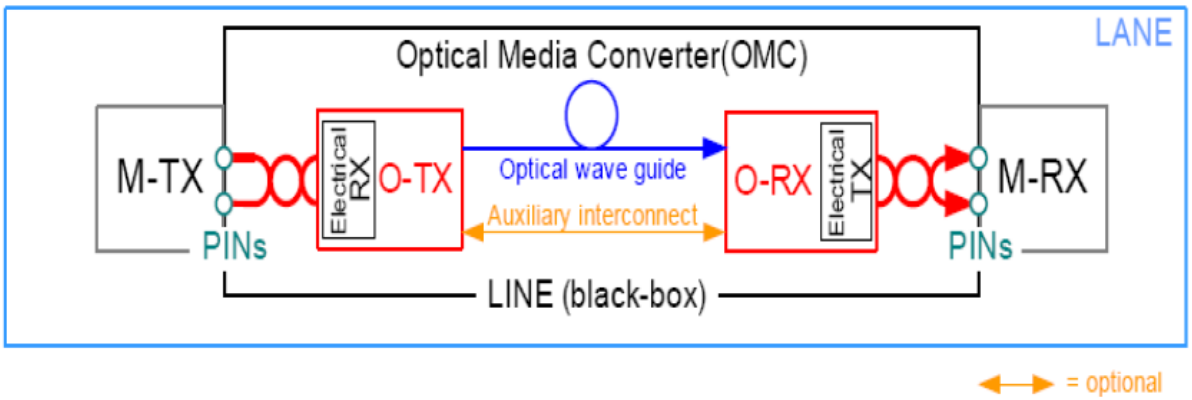

Figure 10: MIPI's Optical Media Converter Module defines an electrical-optical interface for Mobile Devices / Source: MIPI Alliance

Although the absolute dates might have to be adjusted to reflect the reality of the standardization process, the current M-PHY road map, depicted in Figure 11, provides the ecosystem with a time line that enables stakeholders to plan for the long term.

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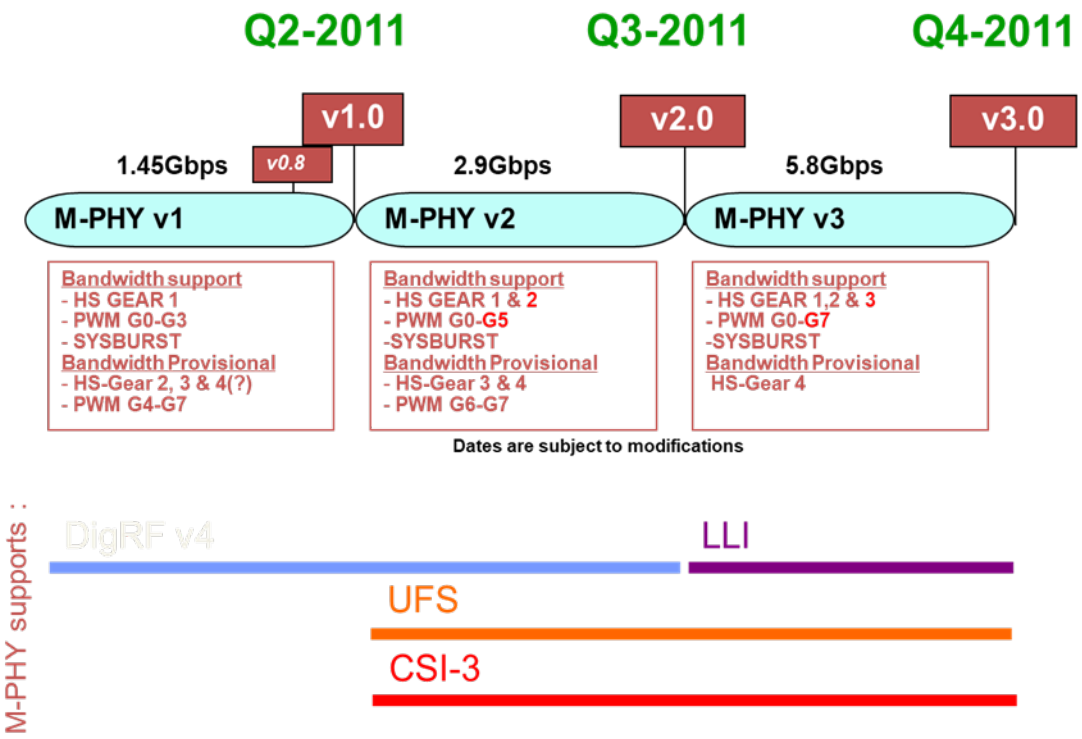

Figure 11: M-PHY roadmap / *Source: STE*

Both ST-Ericsson and Mixel have a wide portfolio of MIPI products, lead the development of the M-PHY specifications and products, and make a significant investment in supporting M-PHY ecosystem.

Conclusion

Due to its unprecedented versatility, the M-PHY is enjoying a wide adoption rate in many applications, some beyond the traditional mobile domain. With this versatility come a large number of benefits and challenges. The M-PHY ecosystem stakeholders, such as semiconductor companies and Intellectual Property (IP) providers will need to overcome the significant challenges that are inherent to this exciting technology are bound to reap the many benefits that it offers. This is paving the way for the system vendors to easily deploy this technology in exciting new products that keeps the end customer captivated, wanting to come back for more.

For information about Mixel's IP portfolio, visit mixel.com/ip-cores.

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[i] Encyclopedia
http://encyclopedia2.thefreedictionary.com/plesiochronous
[ii] Encyclopedia
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[iii] M-PHY Takes Center Stage
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