Mixed-Signal Excellence

Dual Mode C-PHY/D-PHY: Enabling Next Generation of VR Displays

About the Authors

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For many years, Virtual Reality (VR) and Augmented Reality (AR) were strongly linked to gaming and entertainment applications. Today, the VR/AR and their combined version, Mixed Reality (MR), have their applications extended to other domains like healthcare, military, education, manufacturing, retail, marketing and advertising. What are the challenges for next generation VR displays? What makes the MIPI® interfaces the best fit for VR/AR/MR applications? What does Mixel, Inc. do to combine the different MIPI PHY offerings into a unique, differentiated, flexible solution? The answers to these questions will be unveiled throughout this article.

To support the diversified applications and use cases of VR, and to address the growing demand to drive VR displays from PCs, cellphones and portable devices, the next generation of VR displays is advancing in many ways compared to the current generation.

The first generation of VR displays supported 1k x 1k resolution, which wasn't enough to display high resolution image in the near field of view. The next generation VR displays are targeted to support display resolutions of ~1000 Pixel Per Inch (PPI) to enable a minimum display resolution of 2k x 2k, all the way up to 4k x 4k providing the best user experience.

Another aspect targeted by the next generation of VR displays is responsiveness, where the LCD crystals must be stabilized before the user is viewing them, to present crisp LCD images in the near field of view. One of the techniques to achieve this, is to load the pixels in, allow some time for them to settle, then flash the backlight so that the user only views the pixels after they are stable. To accomplish this, the display panel must be updated at faster rates which translates to higher bandwidth requirements.

Lowering video latency is one more challenge. A high video latency results in video content lag which can lead to video and audio contents getting out of sync. Such effects lead to motion sickness issues. The next generation of VR display ICs should be optimized for lowest latencies, which requires deploying low latency interfaces.

The increase in bandwidth to support greater resolutions, higher refresh rates, and faster responsiveness, can't take place without keeping an eye on the power consumption. Commonly deployed in immersive head mounted displays, VR devices should consume minimal power resulting in negligible heat generation for convenient user experience. In applications where the displays are driven from a cell phone or other portable devices, minimizing power dissipation continues to be a key requirement. While all standardized interfaces compete to achieve highest bandwidth, MIPI specifications are developed from the ground up to support high bandwidth, low latency applications, while minimizing power consumption.

MIPI in XR System

The term XR is commonly used to refer to any of the reality technologies VR, AR and MR or any combination thereof. Now, let us take a quick look at MIPI C-PHY℠ and D-PHY℠ interfaces, explain why they represent the optimum choice for XR applications, and how Mixel combined the features of both interfaces in single PHY with minimum area and power overhead.

The MIPI D-PHY is a simple source synchronous PHY that uses one clock lane and a varying number of data lanes. It has been around since 2009, and widely deployed in CSI-2℠ and DSI℠ applications. The C-PHY, on the other hand, is a newer member of MIPI family and a more complex PHY. The C-PHY operates on three signals, a trio, and the clock is embedded into the data, rendering a separate clock lane unnecessary. The single-lane D-PHY 1.2 configuration requires four pins, two pins for clock lane and two pins for data lane, achieving data rate up to 2.5 Gbps. A single-trio C-PHY 1.1 configuration requires only three pins, achieving symbol rates up to 2.5 Gsps which translates to 5.7 Gbps. Thanks to MIPI C-PHY clever and efficient mapping and encoding techniques, the data rate efficiency is multiplied by a factor of 2.28.

To explain the different use cases of MIPI D-PHY and MIPI C-PHY in VR, AR and MR systems, let's look at Figure 1.

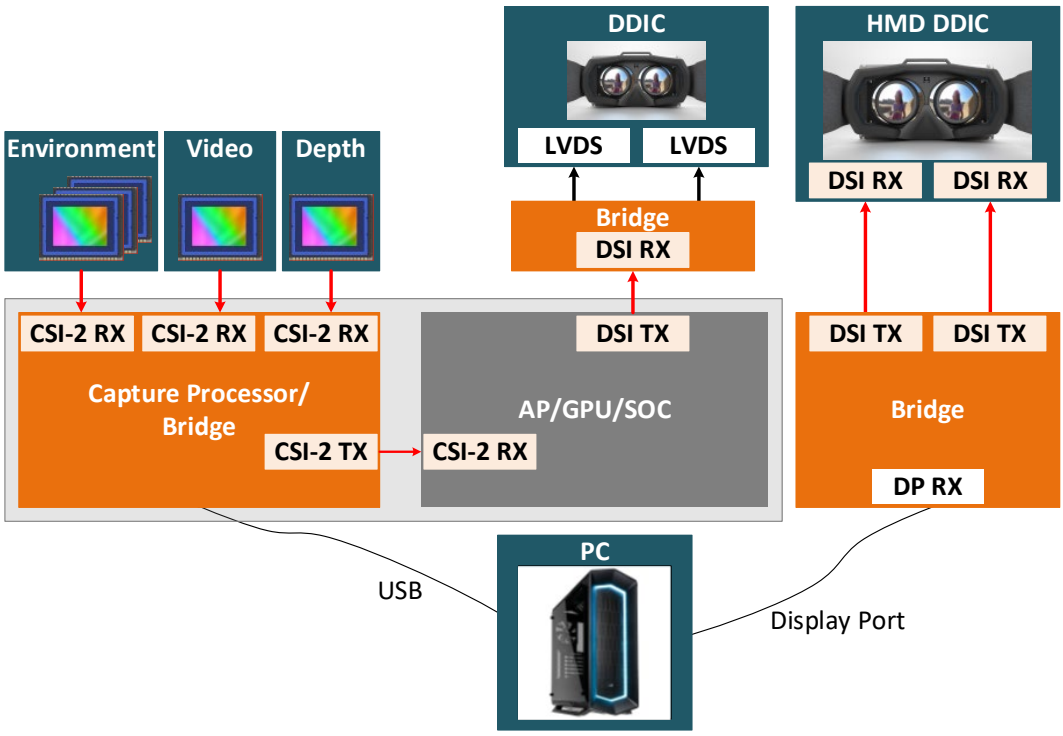

Figure 1: MIPI Use Cases in XR System

The MIPI CSI-2 interface is commonly used for AR applications as an interface between different types of sensors (environment, video capture, depth capture) on one side and a capture processor or bridge chip on the other side. The DSI interface is typically used in VR applications in which a GPU processor will be driving a display panel. The interface between capture processor and the main host processor can deploy another pair of MIPI TX/RX low latency PHY's. In tethered applications, where a non MIPI interface is used by the processor (cell phone, desktop or laptop), a bridge chip can be deployed to convert the data to MIPI form. Both DSI and CSI-2 are MIPI protocols that can send data over MIPI C-PHY and/or MIPI D-PHY physical layers.

Mixel's Dual Mode C-PHY/D-PHY

Mixel's dual mode C-PHY /D-PHY implementation combines both into a combo PHY while sharing the same pads. The D-PHY link can operate as 1 to 4 lanes, each running at 2.5Gbps and the C-PHY link can operate as 1 to 3 lanes, each running at up to 2.5Gbsps, which is equivalent to 5.7Gbps. The Mixel Combo PHY supports aggregate data rate of up to 10 Gbps in the D-PHY mode, and 17.1Gbps in the C-PHY mode

The combo PHY IP not only shares the serial interface pins, but Mixel's implementation also reuses all the MIPI D-PHY functional blocks for the MIPI C-PHY, minimizing die

area and leakage power. Figure 2 below shows the block diagram of Mixel MIPI C-PHY/D-PHY Combo TX for DSI host applications designed to drive latest VR displays.

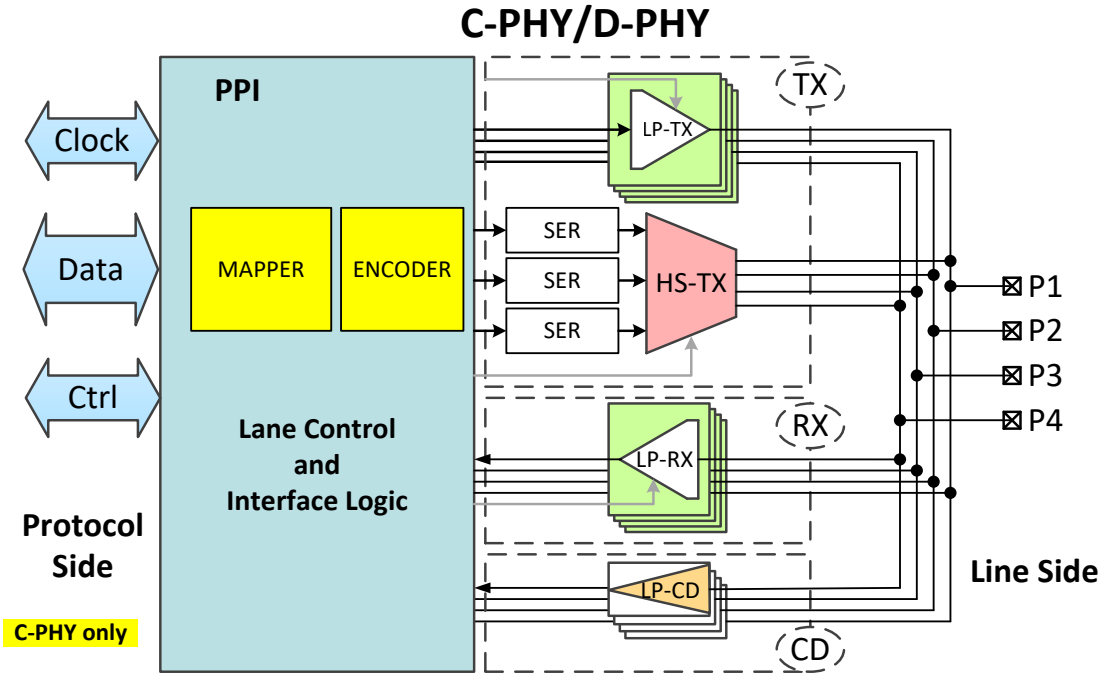

Figure 2: Mixel MIPI C-PHY/D-PHY Combo TX Block Diagram

Mixel Combo C-PHY/D-PHY supports lane swapping and polarity change features in both D-PHY and C-PHY modes. With such a feature in place, system integration and PCB routing are much smoother because lanes/trio can be configured to multiple combinations.

It also equipped with built-in-self-test (BIST) engine enable testing of the PHY across several layers of abstraction (IC, PCB, etc.). The BIST engine is capable of testing the Combo PHY in different MIPI modes of operation with improved observability and controllability. A variety of test scenarios is implemented to enable both production and characterization testing.

Synaptics' Use-Case

Deploying Mixel C-PHY/D-PHY Combo TX Solution, Synaptics Incorporated, a leading provider of high-tech human interface solutions, developed the world's first display applications IC using both MIPI C-PHY and D-PHY. The VXR7200 VR Bridge is a connectivity solution for tethered USB Type-C cables deploying full VESA DP1.4 bandwidth. It is optimized for VR, AR, and MR dual displays headsets with resolutions up to 3k x 3k @ 120Hz with DSC compression to achieve best-in-class HMD user

experience. The Synaptics R63455 VR Display Driver IC is a companion chip that drives displays using special VR display timing modes.

The VXR7200 VR Bridge chip manages both DisplayPort and MIPI sides of the bridge. It communicates through a Display Port interface with the GPU processor to provide display requirements like video formats (Sub-Pixel Render, 420, 444, 8-bit, 10-bit), compression settings and frame timing allocation. On the other side, Mixel MIPI C-PHY/D-PHY and DSI-2 controller are used to communicate with the display driver IC (DDIC) to configure video formats, compression settings, panel scan time, settle time, backlight flash time and local dimming settings.

By integrating two instances of Mixel Combo C-PHY/D-PHY and DSI-2 controller per link, the bridge chip MIPI interface is extended to support eight MIPI D-PHY data channels sharing the same chip pins with six MIPI C-PHY trios per eye. The bridge MIPI interface is highly configurable to support different generations of display panels, multiple resolution and bandwidth options, and variant compression settings. Table 1 below explains why dual mode dual-mode C-PHY/D-PHY interface is required to support wide variety of applications and configurations.

Parameter	No Compression	2:1 Compression Bridge to Display	2:1 Compression GPU to Display	3:1 Compression GPU to Display	2880x1920 Display
MIPI data/line (bytes)	10,710	6,390	6,390	4,950	Per Eye
Minimum MIPI C-PHY link	6-trio C-PHY	4-trio C-PHY	4-trio C-PHY	3-trio C-PHY	Per Eye
Minimum MIPI D-PHY link	-	8-lane D-PHY	8-lane D-PHY	8-lane D-PHY	Per Eye
DP data/line (bytes)	17,808	17,808	8,904	5,936	Host I/F
DP total bandwidth (Gbps)	32	32	16	11	Host I/F
Minimum DP link	4-lane HBR3	4-lane HBR3	4-lane HBR2	2-lane HBR3	Host I/F

Table 1: Bridge Chip Data Rates Supported in Different Configurations

The table above shows examples of different configurations to drive 2880x1920 at 90Hz display per eye. With no compression, the DP link must be configured to 4-lane HBR3 supporting 32Gbps bandwidth, this has to be matched with 6 C-PHY trios on the MIPI interface side to drive the 2880x1920 per eye display. The D-PHY cannot used in this because its max supported bandwidth is below the system requirement in such a configuration. C-PHY support was required to support this important feature.

When either bridge to display or GPU to display compression is enabled, it is possible to use different configurations of D-PHY lanes or C-PHY trios to deliver the required MIPI bandwidth with optimized power consumption.

Silicon Results

Below are two snapshots showing the test results of Mixel dual-mode C-PHY/ D-PHY integrated into Synaptics VXR7200 VR Bridge IC. Achieving first time silicon success with Mixel Combo PHY IP and DSI-2 controller, the VXR7200 Bridge Chip went to production, and is now available in market.

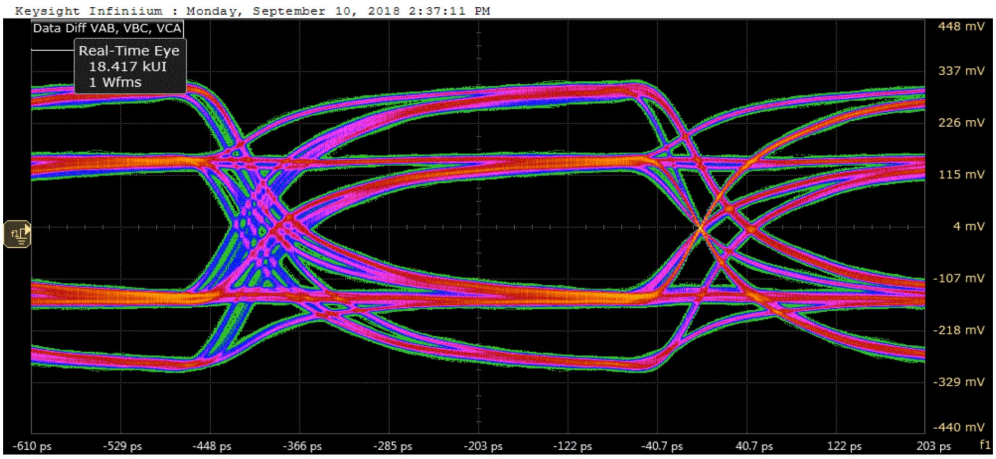

Figure 3: Mixel MIPI C-PHY Eye Diagram at 2.5Gsps

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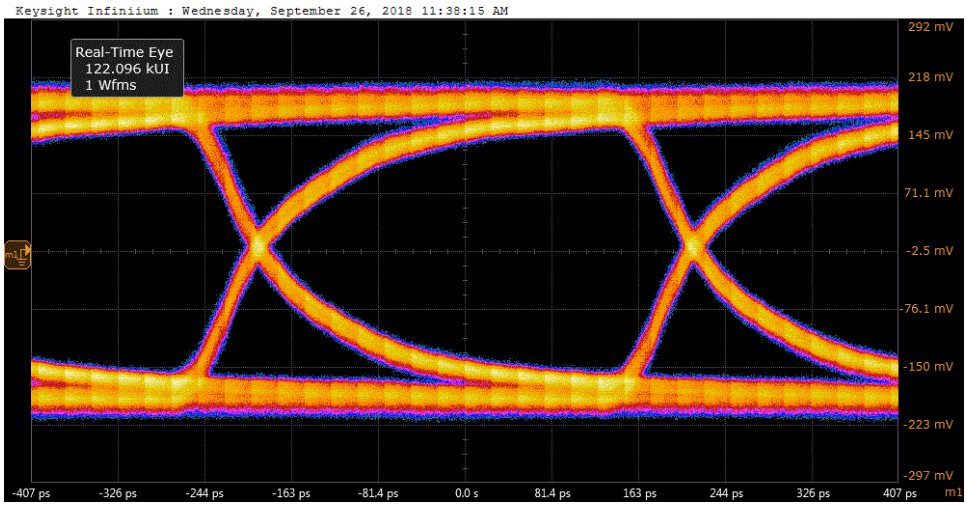

Figure 4: Mixel MIPI D-PHY Eye Diagram at 2.5Gbps

In summary, the VR/AR/MR applications are growing and emerging in different domains with increased demand to support higher bandwidths with minimal power consumption, latency, and EMI. MIPI interfaces attributes are perfectly suited for the XR applications requirements. Mixel dual-mode C-PHY/D-PHY IP offering is unique, flexible and versatile solution for both system bring-up and application use-cases. The multiple link configurations supported by Mixel C-PHY/D-PHY product make it the ideal choice for all XR display and sensor applications.

For information about Mixel's IP portfolio, visit mixel.com/ip-cores.