Feature:

- Complies with MIPI Standard for D-PHY V 1.0
- Point-to-point differential interface supporting multiple data lanes and a clock lane
- Supports both high speed and low-power modes
- Data lanes support both bidirectional and unidirectional modes
- Clock lane supports unidirectional communication
- 80 Mbps to 1Gbps data rate in high speed mode
- 10 Mbps data rate in low-power mode
- Modular design to allow for all possible configurations
- Low power dissipation

General Description:

The MXL-PHY-MIPI is a high-frequency low-power, low-cost, source-synchronous, physical Layer compliant with the MIPI Alliance Standard for D-PHY. Although it is primarily used for connecting cameras and display devices to a host processor, it can also be used for many other portable applications. It is used in a master-slave configuration. High-Speed signals have a low voltage swing, while Low-Power signals have large swing. High-Speed functions are used for High-Speed Data traffic while low power functions are mostly used for control.

Block Diagrams:

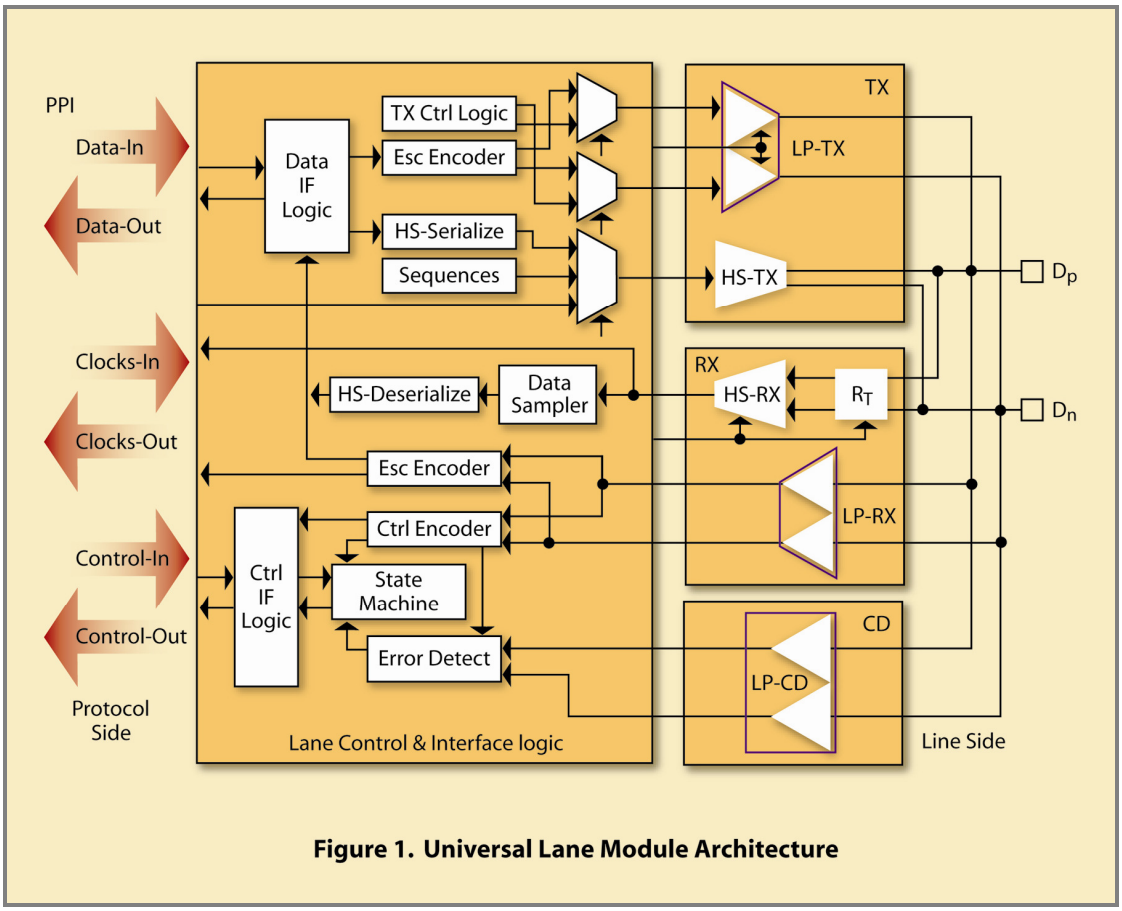

Figure 1. Universal Lane Module Architecture

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