Features:

- 25-180 MHz clock support
- Up to 1.25 Gbps bandwidth
- Up to 5.0 Gbps data throughput
- Low power CMOS design
- Power Down mode
- Low swing LVDS devices for low EMI
- PLL requires no external components
- 1.8V/3.3V dual power supply
- 7/10 bit programmable parallel data transmitted per pixel clock per cannel
- Compatible with TIA/EIA-644 LVDS Standard

General Description:

The MXL-LVDS-RX-4CH is a high performance 4-channel LVDS De-serializer implemented using digital CMOS technology. Both the serial and parallel data are organized into four channels. The parallel data can be 7 or 10 bits wide per channel. The input clock is 25MHz to 180MHz. The Receiver is highly integrated and requires no external components. Great care was taken to insure matching between the Data and Clock channels to maximize the receiver margin. The circuit is designed in a modular fashion and desensitized to process variations. This facilitates process migration, and results in a robust design.

Block Diagram:

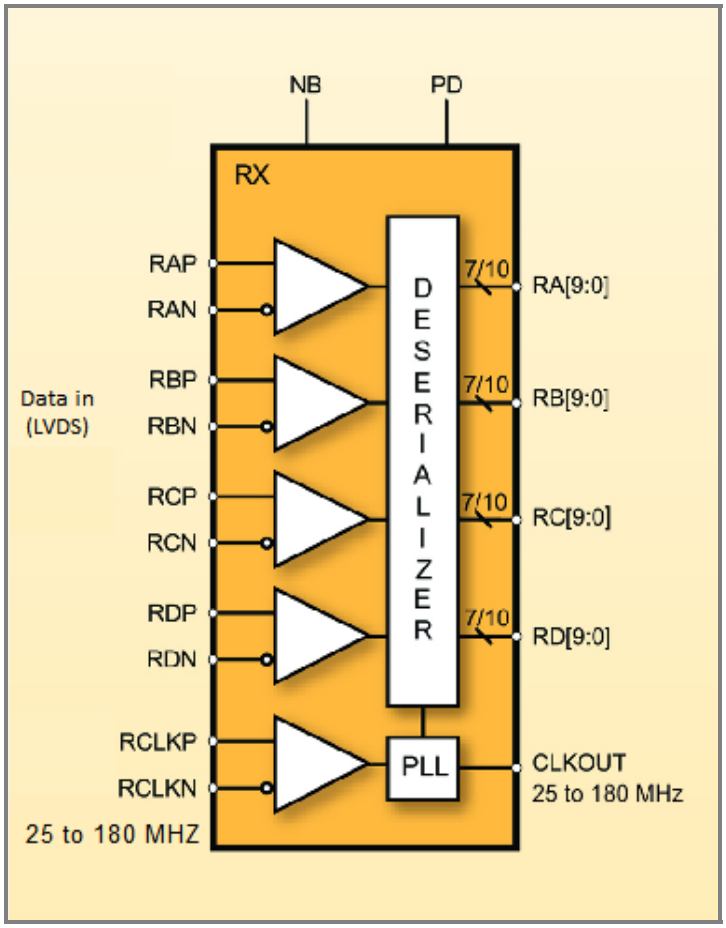

Figure 1: LVDS 4 channel deserializer block diagram

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