1 Features

- Dual mode PHY can support C-PHY℠ and D-PHY℠
- Supports MIPI® Specification for D-PHY Version 1.2
- Backward compatible with MIPI® Specification for D-PHY Version 1.1
- Supports MIPI® Specification for C-PHY Version 1.0
- Four Lane in D-PHY mode
- Three Lane in C-PHY mode
- Supports both high speed and low-power modes
- 80 Mbps to 2.5 Gbps data rate in high speed D-PHY mode
- 80 Msps to 2.5 Gsps data rate in high speed C-PHY mode
- 10 Mbps data rate in low-power mode
- Low power dissipation
- Testability support
- Optional resistance termination calibrator

2 General Description

The MXL-CPHY-DPHY-DSI-TX is a high-frequency low-power, low-cost, source-synchronous, physical Layer. The PHY is configured as a MIPI Master supporting display interface DSI. The High-Speed signals have a low voltage swing, while Low-Power signals have large swing. High-Speed functions are used for High-Speed data traffic while low power functions are mostly used for control.

3 Block Diagram

The block diagrams in D-PHY and C-PHY modes are shown in Figure 1 and Figure 2.

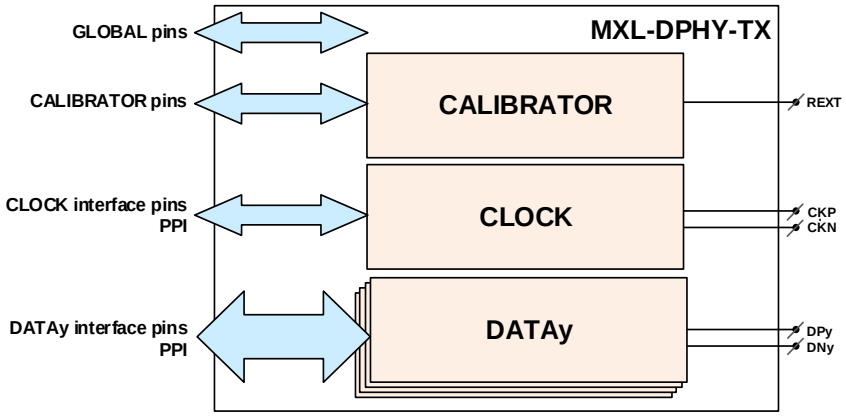

Figure 1: MIPI D-PHY TX Block Diagram