Mixel IP Cores MIPI® D-PHY℠ TSMC 16nm FFC 0.8V/1.8V
Specification Document

1 Features

- Supports MIPI® Specification for D-PHY Version 1.2.
- Optimized for Automotive applications.
- Fully functional -40°C to 150°C Tj.
- Designed to achieve CPK of 2.0 across PVT.
- One Clock Lane and Four Data Lanes.
- Supports both high speed and low-power modes.
- 80 Mbps to 1.5 Gbps data rate per lane without DeSkew calibration.
- Up to 2.5 Gbps data rate per lane with DeSkew calibration.
- 10 Mbps data rate in low-power mode.
- Low power dissipation.
- Loopback testability support.
- Optional resistance termination calibrator.

2 General Description

The MXL-DPHY-UNIV is a high-frequency low-power, low-cost, source-synchronous, physical Layer supporting the MIPI Alliance Specification for D-PHY v1.2.
The IP can be configured as a MIPI Master or MIPI Slave optimized for CSI-2℠ (Camera Serial Interface), and DSI℠ (Display Serial Interface) applications.
The High-Speed signals have a low voltage swing, while Low-Power signals have large swing. High-Speed functions are used for High-Speed data traffic while low power functions are mostly used for control.

The D-PHY supports a bit rate range of 80 to 1500 Mbps per Lane without deskew calibration and up to 2500 Mbps with deskew calibration.
The maximum data rate in low-power mode is 10 Mbps. For a fixed clock frequency, the available data capacity of a PHY configuration can be increased by using more lanes. Effective data throughput can be reduced by employing burst mode communication.

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3 Block Diagram

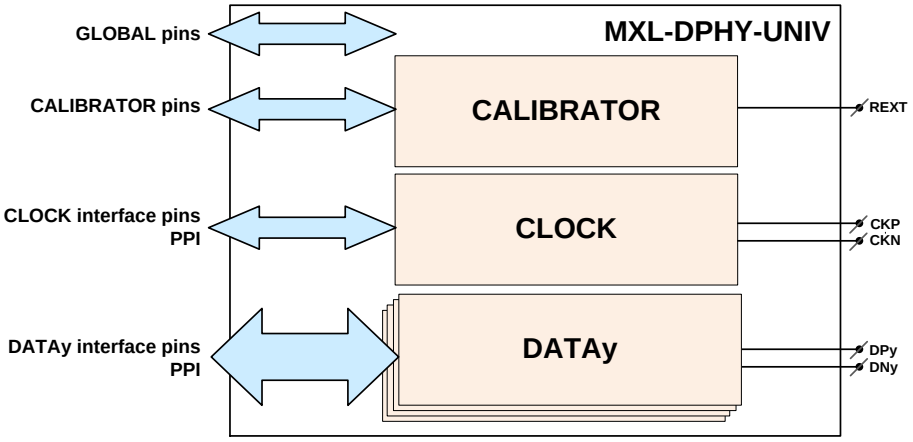

Figure 1: MIPI D-PHY Universal Block Diagram

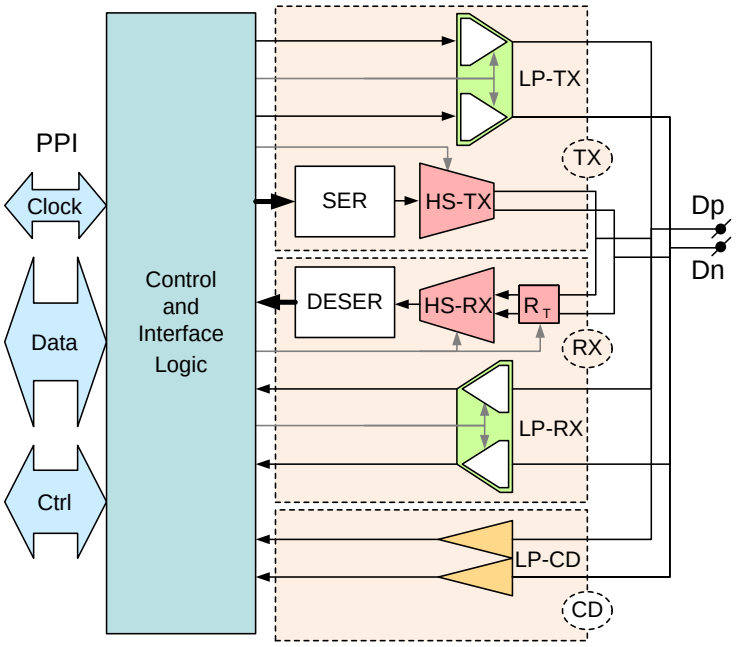

Figure 2: Universal Lane Overview