1   Features

- Consists of 1 Clock lane and up to 4 Data lanes
- Supports MIPI® Alliance Specification for D-PHY℠ Version 1.1
- Supports both high speed and low-power modes
- 80 Mbps to 1.3 Gbps data rate in high speed mode
- 10 Mbps data rate in low-power mode
- High Speed Deserializers included
- Low power dissipation
- Testability support
- Optional resistance termination calibrator

2   General Description

The MXL-DPHY-DSI-RX is a high-frequency low-power, low-cost, source-synchronous, Physical Layer supporting the MIPI Alliance Specification for D-PHY v1.1.
The IP is configured as a MIPI Slave optimized for DSI℠ (Display Serial Interface) applications.
The High-Speed signals have a low voltage swing, while Low-Power signals have large swing. High-Speed functions are used for High-Speed data traffic while low power functions are mostly used for control.
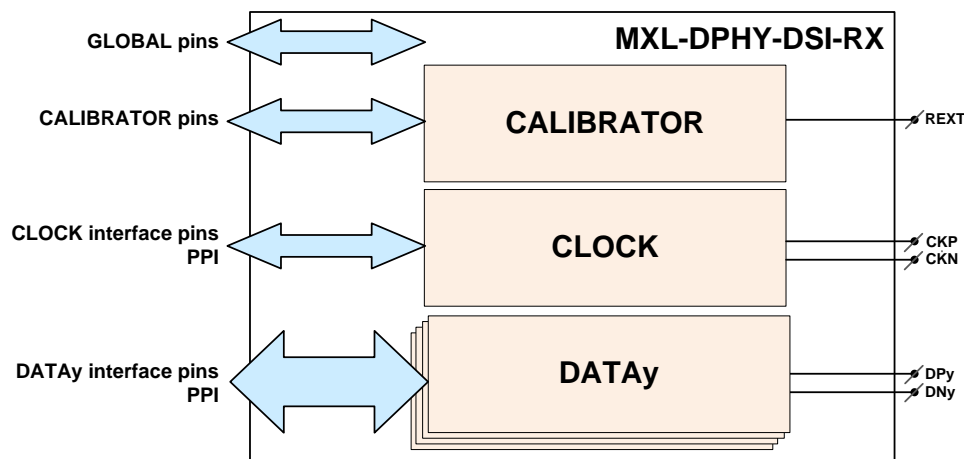
3   Block Diagram

Figure 1: MIPI D-PHY Block Diagram