1 Features

- Consists of 1 Clock lane and up to 4 Data lanes
- Supports the MIPI Standard 1.1 for D-PHY
- Supports both high speed and low-power modes
- 80 Mbps to 1.5Gbps data rate in high speed mode
- 10 Mbps data rate in low-power mode
- High Speed Serializers and Deserializers included
- Low power dissipation
- Loopback testability support
- Optional resistance termination calibrator

2 General Description

The MXL-DPHY-UNIV is a high-frequency low-power, low-cost, source-synchronous, Physical Layer that supports the MIPI® Alliance Standard for D-PHY.
The IP can be configured as a MIPI Master or MIPI Slave optimized for camera interface (CSI-2) and display (DSI) applications.
The High-Speed signals have a low voltage swing, while Low-Power signals have large swing. High-Speed functions are used for High-Speed data traffic while low power functions are mostly used for control.

3 Block Diagram

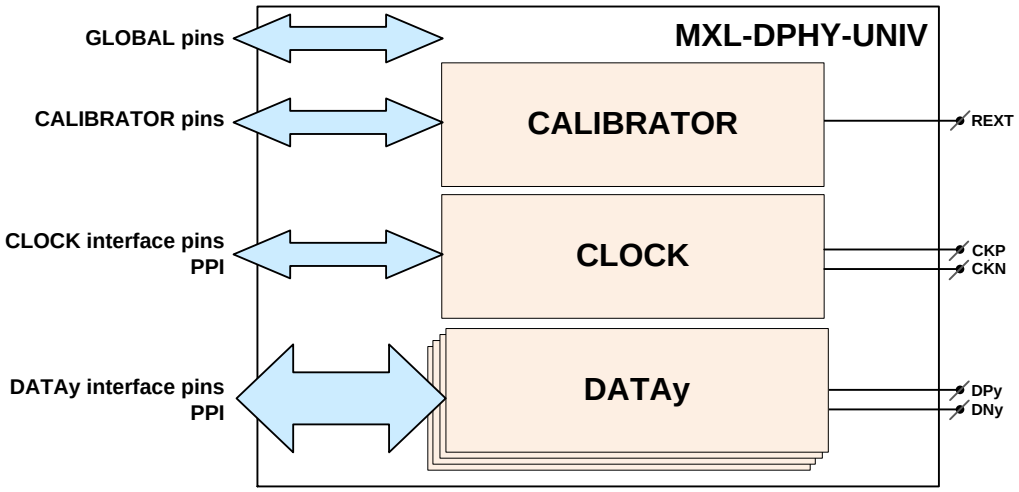

Figure 1:MIPI D-PHYUniversalBlock Diagram

Mixel, Inc.
97 E. Brokaw Road, Suite 250, San Jose, CA 95112
Ph.: (408) 436-8500, Fax: (408) 436-8400
www.mixel.com