1 Features

- Dual mode PHY can support C-PHY and D-PHY
- Supports MIPI Specification for D-PHY Version 1.2
- Supports MIPI Specification for C-PHY Version 1.0
- Four Lane in D-PHY mode
- Three Lane in C-PHY mode
- Supports both high speed and low-power modes
- 80 Mbps to 2.5 Gbps/Gsps data rate in high speed mode
- 10 Mbps data rate in low-power mode
- Low power dissipation
- Loopback testability support
- Optional resistance termination calibrator
- Deskew calibration support in D-PHY

2 General Description

The MXL-CPHY-DPHY-UNIV is a high-frequency low-power, low-cost, source-synchronous, physical Layer. The PHY can be configured as a MIPI Master or MIPI Slave supporting camera interface CSI-2 v1.2 and display interface DSI v1.3 applications in the D-PHY mode. It also supports camera interface CSI-2 v1.3 and display interface DSI-C v1.0 applications in the C-PHY mode. The High-Speed signals have a low voltage swing, while Low-Power signals have large swing. High-Speed functions are used for High-Speed data traffic while low power functions are mostly used for control.

3 Block Diagram

The block diagrams in D-PHY and C-PHY modes are shown in Figure 1 and Figure 2.Figure 1

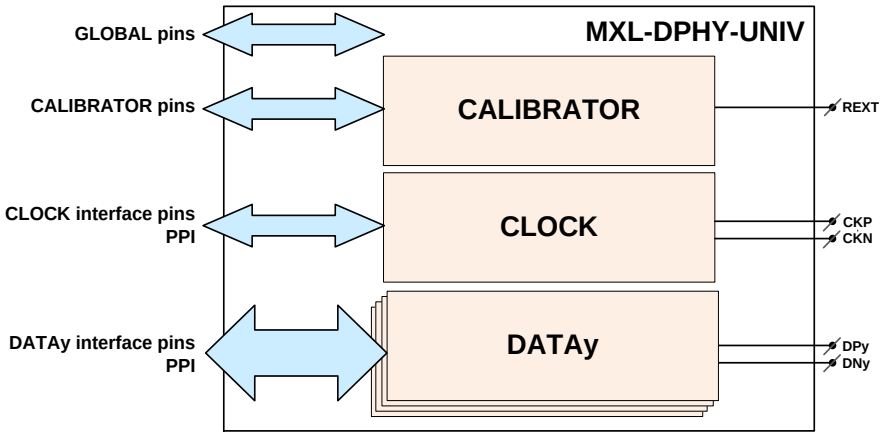

Figure 1: MIPI D-PHY Universal Block Diagram