1. Features

- Consists of 1 Clock lane and up to 4Data lanes
- Supporting the MIPI Standard 1.1 for D-PHY
- Supports both high speed and low-power modes
- 80 Mbps to 1.5Gbps data rate in high speed mode
- 20 Mbps data rate in low-power mode
- High Speed Deserializers included
- Low power dissipation

2. General Description

The MXL-PHY-DSI-RX is a high-frequency low-power, low-cost, source-synchronous, Physical Layer supporting the MIPI Alliance Standard for D-PHY.
The IP is configured as a MIPI slave optimized for display interface applications (DSI).
The High-Speed signals have a low voltage swing, while Low-Power signals have large swing. High-Speed functions are used for High-Speed Data traffic while low power functions are mostly used for control.

3. Block Diagram

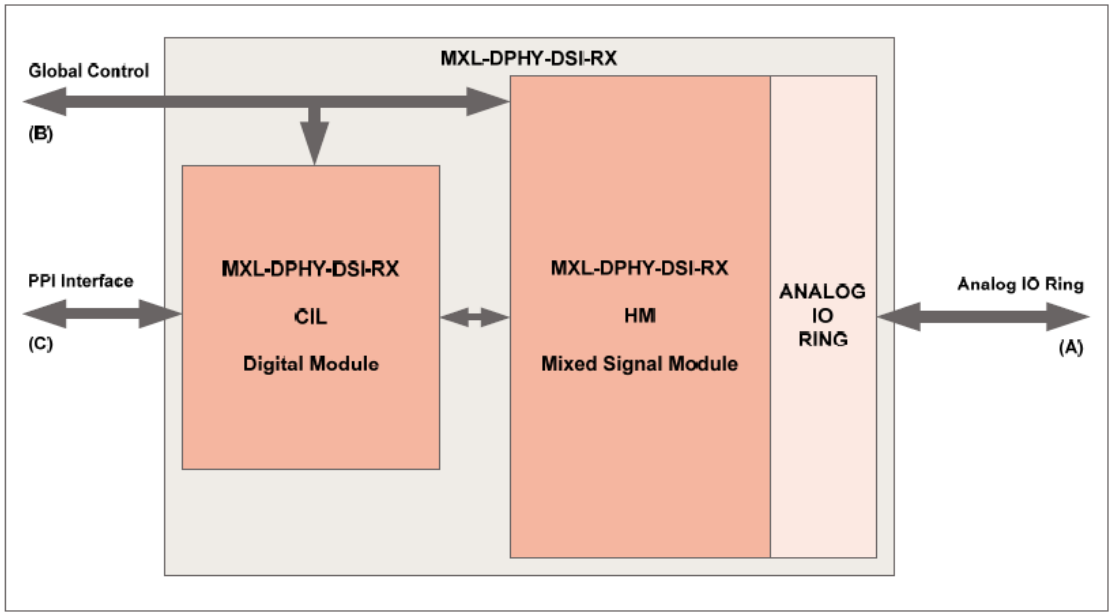

Figure 1 – MIPI DPHY DSI-RXBlock Diagram

Mixel, Inc.
97 East Brokaw Road, Suite 250, San Jose, CA 95112
Ph.: (408) 436-8500, Fax: (408) 436-8400
www.mixel.com