Features:

- Consists of 1 Clock lane and 3 Data lanes
- Complies with MIPI Standard 1.0 for D-PHY
- Supports both high speed and low-power modes
- 80 Mbps to 1Gbps data rate in high speed mode
- 10 Mbps data rate in low-power mode
- High Speed Serializer and Deserializer included
- Include circuitry for production test
- Low power dissipation

General Description:

The MXL-PHY-DSI-TX is a high-frequency low-power, low-cost, source-synchronous, Physical Layer compliant with the MIPI Alliance Standard for D-PHY.

The IP is configured as a MIPI master and consists of 4 lanes: 1 Clock lane and 3 data lanes, which makes it suitable for display interface applications (DSI).

The High-Speed signals have a low voltage swing, while Low-Power signals have large swing. High-Speed functions are used for High-Speed Data traffic while low power functions are mostly used for control.
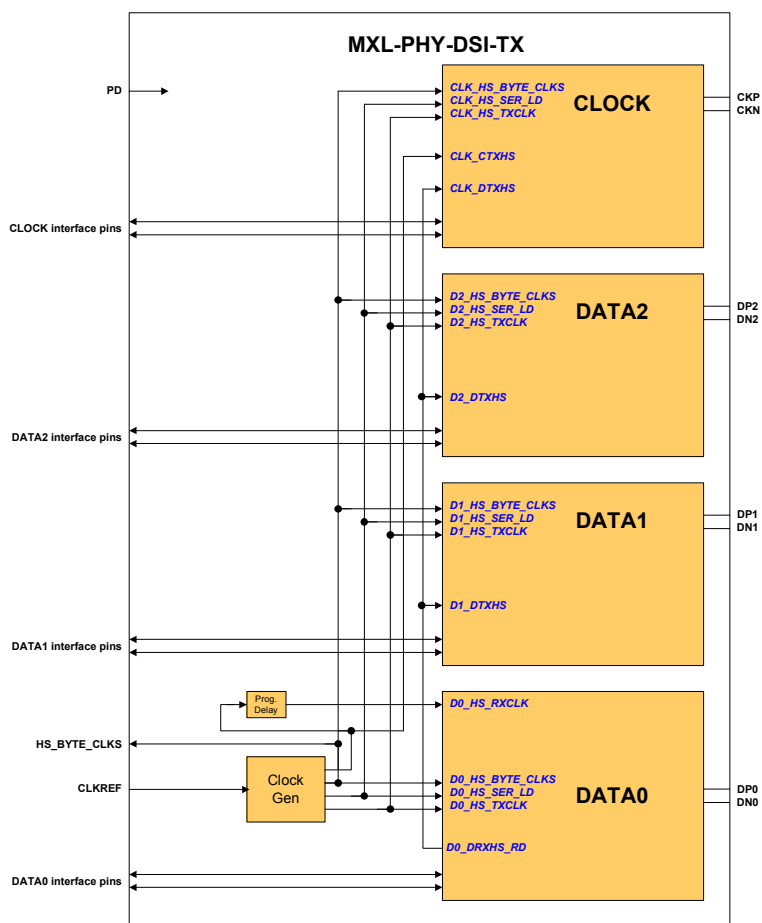
Block Diagram:

Figure 1 – PHY Block Diagram